An integrated single photon detector array using porous anodic alumina

Joost Melai, Cora Salm, Jurriaan Schmitz, Sander Smits and Jan Visschers

Abstract—**This paper outlines a single photon sensitive detector array. The detector structure is made via CMOS compatible wafer-scale post-processing. The total system comprises a CMOS imaging chip with charge sensitive pixels, an electron multiplier and a photo-cathode. The electron multiplication is achieved by operating a thick layer of integrated porous anodic alumina as an MCP. Material and geometry considerations are given as well as some first experimental results on the required processing steps and on an intermediate experiment with discrete samples of porous anodic alumina.**

Index Terms—**CMOS compatibility, electron multipliers, Micro-Channel Plate, photon detection, porous anodic alumina, waferscale post-processing**

I. Introduction

The aim of this work is the fabrication of a photon detector array, sensitive to single photons, made using IC compatible wafer-scale post-processing steps.

The detector comprises a photo-cathode, an electron multiplication structure and an imaging chip which serves as a smart substrate for the system. Figure 1 shows the three components separately. The imaging chip that will be used is Medipix2 [1], [3], it consists of 256×256 pixels at a pitch of 55 µm. Each pixel contains a charge sensitive pre-amplifier. An incoming photon will be converted into a photo-electron by the photo-cathode, this primary electron is multiplied into a space charge of several thousand electrons in the electron multiplication structure. The accumulated charge at the bottom of the structure is transferred directly to the charge sensitive input pads of the imaging chip underneath. Figure 1 illustrates the working principle, the whole assembly is operated in vacuum. It is very similar to existing photo-multiplier tube applications and also for instance to the system described in [2]. The main difference is that the whole system is integrated on a high resolution imaging chip rather than constructed of discrete elements.

The system is made using standard CMOS processing for the imaging chip and CMOS compatible wafer-scale post-processing for the rest. In order not to harm the IC the post-processing needs to respect the CMOS vulnerabilities for high temperature, stress, charging due to plasma processing, metal contamination and loss of hydrogen passivation.

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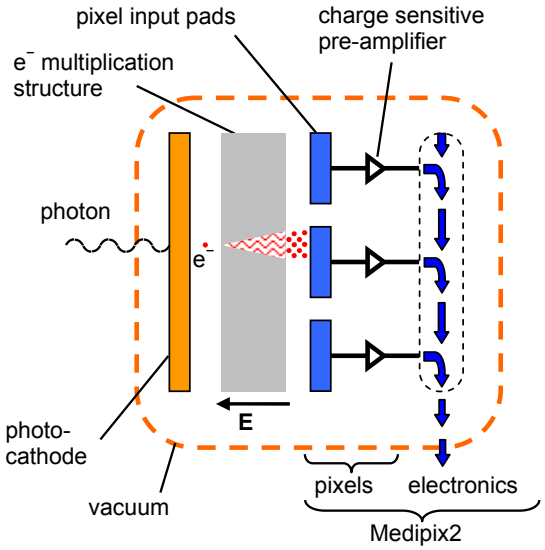

Figure 1: Overview of the system, showing the three parts: photo-cathode, electron multiplication structure and a pixellized imaging chip. This image shows 3 pixels, in reality the system is based on a large rectangular array of pixels.

The electron multiplication structure consists of a thick layer of porous alumina (Al_2O_3) that acts as an integrated Micro-Channel Plate (i-MCP). The MCP is biased with a high potential on the cathode stack placed on top, on the bottom it connects to the grounded anodes of the imaging chip.

After photo-electric conversion the primary electron drifts into one of the pores of the MCP, collision with the sidewall cause an avalanche of secondary electrons, at the bottom the accumulated charge is collected at the input pads of the charge sensitive pixel detector. Due to the design of the pre-amplifier the device is capable of detecting small signal charges (of less than 1000 e^-) in spite of the large bias current that is also fed through the pixel anodes [3].

II. MCP Geometry

To find the optimal pore geometry several things have to be taken into account. First we will look at the basics of MCP operation using a simple gain model known from literature (for instance [4]).

A. Gain model for MCP operation

The total gain, G, of each of the pores is defined by the number of collisions, n, and the amount of secondary electrons created at each collision, δ. This last metric varies with the acceleration voltage the carriers experience between two collision steps, V_{Coll}, and a material dependent constant, A, expressed in $V^{-0.5}$ [4].

$$G = \delta^n$$
$$\delta = A\sqrt{V_{Coll}} \quad (1)$$

If we assume that the pores are straight and that all secondary electrons exit the surface perpendicularly with an energy $q \cdot V_0$, the following expression for G can be derived.

$$G = \left(\frac{A \cdot V}{2 \cdot \alpha \cdot \sqrt{V_0}} \right)^{\frac{4 \cdot V_0 \cdot \alpha^2}{V}} \quad (2)$$

The only remaining geometry factor is the aspect ratio of the pores α. V is the total bias voltage across the MCP. For the following graphs V_0 is assumed to be 1 V and A is 0.2 $V^{-½}$ [4]. Results of this gain model are plotted below in Figure 2.

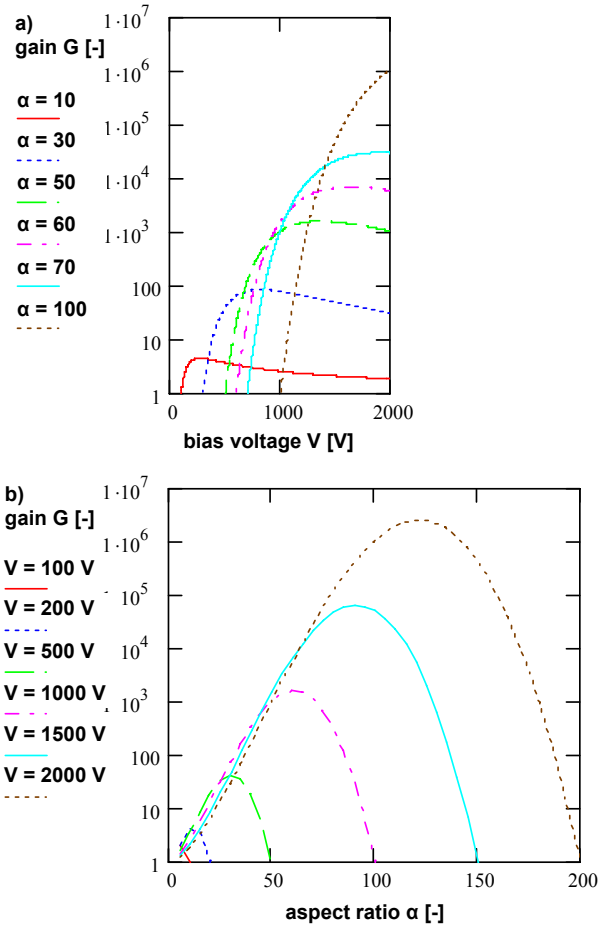

Figure 2: Plots of the gain behavior as found from the model described above, plot a) shows *G* vs. *V* for varying *α*, plot b) shows *G* vs. *α* for varying *V*.

If the pores are too long relative to the diameter (high α) there are too many collisions with only a limited voltage drop per step, this means the electrons do not gain enough energy to create (several) secondary electrons. If the pores are too short relative to the diameter (low α) there will be too little collisions, the electrons travel too far vertically during the time it takes them to traverse the width of the pore.

B. Choice of geometry

From Figure 5a) it can be seen that for a gain > 10^3 a bias voltage of at least 1 kV is needed. At the same time we learn from Figure 5b) that for the same gain requirement the aspect ratio has to be at least 50.

Another consideration is gain saturation, this will limit the minimal pore width. If a too high concentration of carriers develops at the bottom end of the pores the charge repulsion will smother further multiplication, leading to saturation of the gain/diameter ratio, a typical limit is 10^5 -/µm. This indicates that a true Nano-Channel Plate would not work, for a typical gain requirement of 10^3 a minimal diameter of 10 nm is needed.

The pore density depends on the pore pitch and the ordering, if we assume a pore pitch p and hexagonal packing the density of pores, ρ_{pores}, is given by (3).

$$\rho_{pores} = \frac{1}{A_{pore}} = \frac{1}{\frac{1}{2} \cdot \sqrt{3} \cdot p^2} \approx \frac{1.15}{p^2} \quad (3)$$

For a pore pitch of 1 µm this results in a pore density of around $1.5 \cdot 10^8$ -/cm^2. If the pores have an aspect ratio of 50 and a surface sheet resistance of 10^{13} Ω/sq this would lead to a total specific resistance across the MCP of $1.1 \cdot 10^6$ Ω·cm^2. With a bias voltage of $1 \cdot 10^3$ V this leads to a leakage current density of $0.94 \cdot 10^{-3}$ A/cm^2 or 29 nA per Medipix2 pixel of 55×55 µm^2. These values are not unacceptable, they are comparable to discrete MCPs.

Lastly dielectric breakdown of the PAA structure needs to be avoided. The dielectric strength of alumina is around 100 V/µm [5], for bias values of up to 2 kV this means the thickness of the dielectric needs to be at least 20 µm.

Given the considerations above it is decided that the targeted MCP structure has a thickness of 25-50 µm and a pore width of 0.25-1 µm. The pore pitch should be as high as technologically feasible.

III. Technology

As mentioned above the integrated detector structure is made on top of an integrated circuit that contains an imaging chip. We assume this imaging IC is made in a CMOS process (Medipix2 is made in a commercial 0.25 µm foundry process), the full process is completed including Al bondpad formation scratch protection layers and sintering. The exposed charge input bondpads on each pixel are exposed, these will act as anode for the electron multiplication structure.

The electrode multiplication structure will be an MCP made

out of porous alumina. This layer is made by anodically oxidizing a thick layer of Al placed over the Al bondpads. The process is completely IC compatible. On top of the IC wafer a thin counter-electrode and a thick pure Al layer are deposited by sputtering. The wafers are immersed in an acidic solution and a bias is applied between the metal stack and an anodization electrode. The Al is converted into a self-organized porous Al_2O_3 structure that acts as an MCP

Bias is applied to the MCP by means of the grounded anodes below and a cathode above. The cathode stack comprises a reflective Photo-Cathode stack, possibly with protection layer [6], [7].

This last step completes the detector structure. Besides the detector anode the chip has other bondpads, these are needed to power the chip and to communicate with the outside world. These bondpads can remain covered with scratch protection nitride during the post-processing. Later they are accessed by removing the PAA layer around the perimeter of the chip, before or after dicing. This step does not require a very high alignment precision. After dicing the individual chips can be tested and packaged.

A. Anodization process

It is very well known that the main instrument to control pore width and pore pitch is the anodization voltage [8]. Typical ratios of pore width/pitch to voltage are around 2-4 nm/V. This is also found in [9]. PAA formation has previously been used to make photonic crystals, with pore sizes of close to 0.5 µm [9], [10], this is within the useful range for MCPs.

For the anodization process we have used phosphoric acid because this is most compatible with the large pore size needed for electron multiplication [9].

First experimental results are shown in the top-view SEM image in Figure 3.

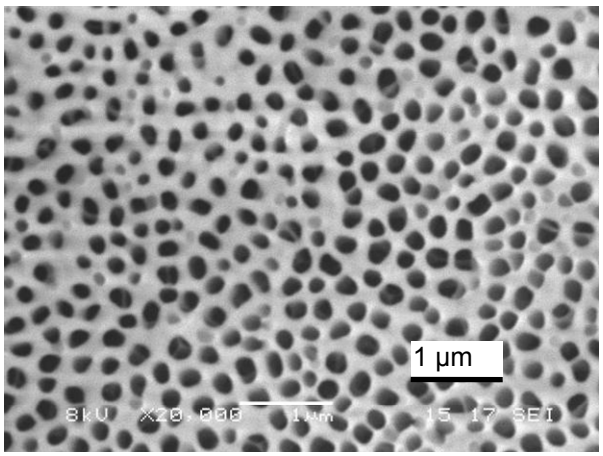

Figure 3: Top-view SEM image of some of the first experimental result with high voltage Al anodization, performed at 150 V in 3 wt% phosphoric acid

The SEM image in Figure 4 shows a cross-section of the PAA film grown from a 10 µm thick Al layer. The Al film has not been converted entirely. The roughness and contrast seen in the unreacted Al is due to deformation during cleaving.

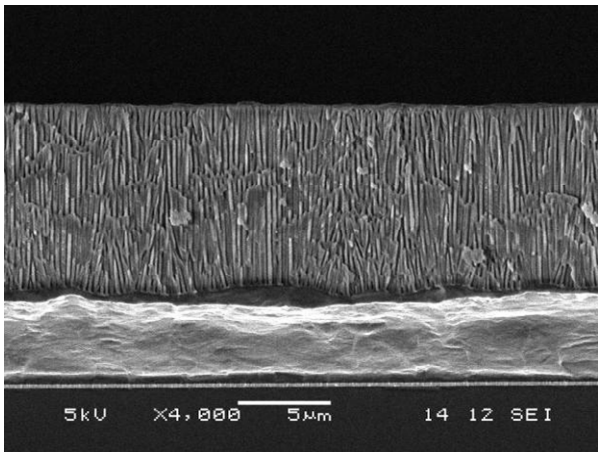

Figure 4: Cross-section SEM image of a partly anodized 10 µm thick Al layer.

B. Integration of compound sub-electrode

To prevent that the anodization process runs through the bondpads (they also consist of Al) a dedicated stopping layer is needed that does not react during anodization. This layer has to be conductive, it also acts as a good electrode so that all of the Al over the whole surface can be converted and no un-reacted pockets of Al are left behind. In Figure 4 it can already be seen that the anodization front is not completely flat, there is a variation in conversion rate.

For this reason a thin W−Ti layer (150 nm, 15 at% Ti) is deposited before the thick Al. The W−Ti layer is compatible with existing processing, it has good sheet resistance (0.4 Ω/□) and it improves adhesion. The W−Ti can be seen in the cross-section image in Figure 4, just above the scale bar.

During anodization a continuous sub-electrode is useful, but after the process is completed and this layer remains it shorts all of the pixels on the chip rendering it useless. The lateral connections need to be removed. The conventional manner of achieving this would be to apply a photolithographic mask and etch selectively the W−Ti layer down to the isolating silicon nitride scratch protection layer in between each pixel. The pixel pattern however is buried below a very thick porous alumina layer. The height difference prohibits aligning a lithographic mask on top of the alumina with the pixel pattern below. Additionally the topography of the layer will present difficulties for most resist processes.

The solution to this is to provide the information on where to etch the W−Ti in a hard-mask layer below the porous alumina. This mask is already deposited and patterned before Al deposition. The mask we will use is a thin layer of Ni, this metal layer is non-reactive (in the atmosphere) providing good adhesion of the Al while it also protects the W−Ti (mostly the Ti) from oxidation. The Ni is patterned to cover the Al anode pads, with a small overlap.

After this the thick Al layer is deposited. The Al is then converted into porous alumina by anodization, this process

stops on the Ni/W−Ti stack. Then the exposed W−Ti is etched, through the pores, selective towards the Ni. The last remaining step is to deposit the cathode stack.

A graphical overview of the process is given in Figure 5 below.

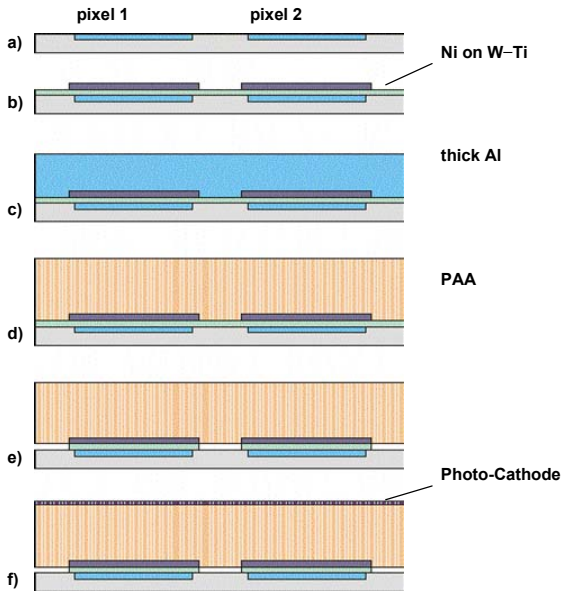

Figure 5: Process flow overview, two pixels are shown, situation after CMOS, only the bondpads in the top metal level are shown (a), patterned Ni on W−Ti (b), deposition of thick Al (c), formation of Porous Anodic Alumina, PAA (d), etch of W−Ti selective towards Ni (e) and deposition of a Photo-Cathode stack (f).

IV. Experimental Results

Conventional MCPs are made form quartz glass, however several groups have previously tried to use (porous) alumina as a dielectric material for MCPs and MCP-like applications [11], [12]. Additionally we have planned several experiments to further prove the validity of using a PAA structure as an MCP.

For some of these experiments discrete disks of PAA are used, these are available commercially, they are normally used for filtering fluids. The disks are 50-60 µm thick, the width of the pores is around 200 nm. Both values show a large variation, over the disk as well as from disk to disk. The aspect ratio varies between 250 and 300.

We have tested the dielectric strength of the PAA disks. The disks have been mounted on a conducting substrate, on the top surface contact areas have been defined of varying size. We have measured the current through the contact areas for varying bias conditions of up to 1500 V. No catastrophic breakdown events have been observed. Figure 6 shows *j-V* curves for the measured devices. There is some variation in the current density from device to device.

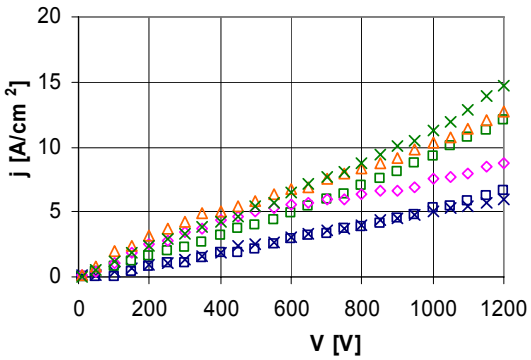

Figure 6: Current density vs. bias voltage for different contact sizes, the PAA disk is 60 µm thick.

By fitting a straight line through the individual IV-curves of the contacts the conductance per device can be found. This conductance is plotted vs. the contact area in Figure 7. A straight line is fitted through the data points to find the specific conductance.

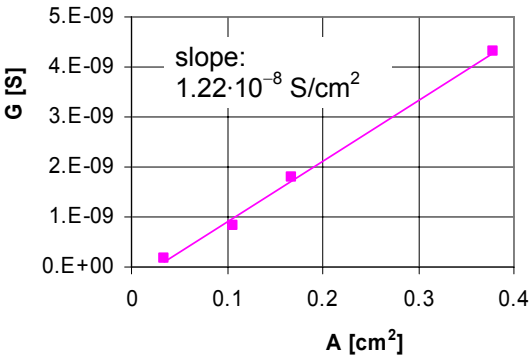

Figure 7: Conductance vs. contact area for one set of samples. The slope of the line fitted through the data points is the specific conductance through the PAA disk.

The specific conductance of the 60 µm PAA disk is $1.22 \cdot 10^{-8}$ S/cm^2, the specific resistance is $8.2 \cdot 10^{7}$ Ω·cm^2.

If we assume this is only due to bulk conduction the resistivity would amount to $1.4 \cdot 10^{10}$ Ω·cm. This however is not likely. We will assume instead that all current will pass along the sidewalls and that bulk conduction is negligible. To find the sidewall conductivity we need to know the sidewall geometry per area. The pore density in our sample is $2 \cdot 10^{9}$ -/cm^2. All of the pores are assumed to be parallel conductances. The conductance per pore can be found to be the specific conductance derived above divided by the pore density. The pore conductance is $6.1 \cdot 10^{-18}$ S, the pore resistance is therefore $1.6 \cdot 10^{17}$ Ω. Each pore, with an aspect ratio of 300, can be viewed as 95 squares in series. The sidewall resistivity is found to be $1.7 \cdot 10^{15}$ Ω/□.

This value is even higher than assumed in the considerations given in section II.B. Furthermore, the measurements were taken at atmospheric pressure, the measurement chamber was flooded with nitrogen but otherwise there was no special conditioning. If the structure is

operated in vacuum the sidewall conductivity is likely to decrease further.

V. Conclusion

A concept has been presented for a single photon sensitive detection system monolithically integrated with a CMOS smart substrate using simple wafer-scale post-processing steps. A processing sequence has been shown to manufacture the system. It involves integrating a Porous Anodic Alumina (PAA) structure that is operated as a Micro-Channel Plate (MCP). Geometry requirements for the integrated MCP have been derived, the targeted MCP structure has a thickness of 25-50 µm and a pore width of 0.25-1 µm. Several processes needed to realize the device have been investigated. Future work will focus on the anodization process, the pores need to be wider and have a larger pore pitch and the process needs to be more reliable.

An intermediate experiment that uses discrete disks of porous anodic alumina has shown that the required biasing can be achieved with the chosen material.

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