Formation of Thick Porous Anodic Alumina Films and Nanowire Arrays on Silicon Wafers and Glass**

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A method for the fabrication of thick films of porous anodic alumina on rigid substrates is described. The anodic alumina film was generated by the anodization of an aluminum film evaporated on the substrate. The morphology of the barrier layer between the porous film and the substrate was different from that of anodic films grown on aluminum substrates. The removal of the barrier layer and the electrochemical growth of nanowires within the ordered pores were accomplished without the need to remove the anodic film from the substrate. We fabricated porous anodic alumina samples over large areas (up to 70 cm^2), and deposited in them nanowire arrays of various materials. Long nanowires were obtained with lengths of at least 9 μm and aspect ratios as high as 300. Due to their mechanical robustness and the built-in contact between the conducting substrate and the nanowires, the structures were useful for electrical transport measurements on the arrays. The method was also demonstrated on patterned and non-planar substrates, further expanding the range of applications of these porous alumina and nanowire assemblies.

1. Introduction

The fabrication of solid-state nanostructures has been motivated by the quantum-size physical phenomena these systems exhibit and by the push to miniaturize computational, electro-optical, and sensing devices. In particular, nanowires are interesting systems in which carriers are confined in the radial dimension, yet transport is possible along the axial dimension of the nanowire.[1] Various fabrication techniques have been developed for the synthesis of nanowires,[2] including template synthesis,[3] the vapor–liquid–solid growth mechanism,[4,5] and sub-micrometer lithography techniques. However, few methods have been developed to organize nanowires into functional structures. General methods for aligning individual nanowires into device-like structures include layer-by-layer fluidic alignment by the use of microfluidic channels[6] and the alignment of metallic nanowires between metal contacts by non-uniform alternating fields.[7] Other approaches are usually sample specific. For example, Yang et al. created patterned arrays of ZnO nanowires by epitaxial growth on a sapphire substrate, controlling the location, the length, and the orientation of the nanowires.[8]

Porous anodic alumina (PAA) has been frequently used for the templated synthesis of nanowires, since this porous template material consists of a self-assembled honeycomb array of uniformly sized parallel channels (see Figs. 1a,b).[9,10] Thus, by

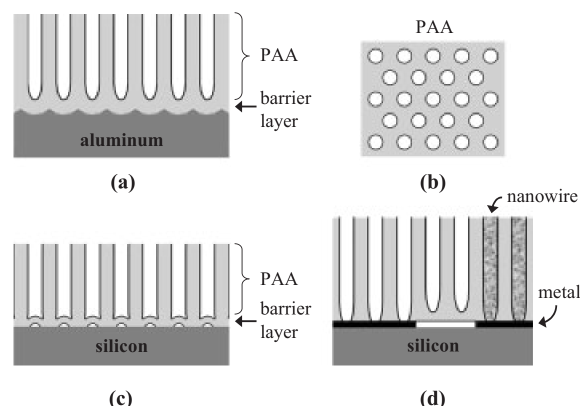

Fig. 1. Schematic representation of the structure of a conventional porous anodic alumina film [a) cross-section; b) top surface]. c) Schematic representation of the structure of a porous anodic alumina film grown on a silicon substrate displaying an inverted barrier layer. d) Schematic representation of the desired structure of a porous alumina film with open channels ending without a barrier layer over metallic films (black strips) patterned on the substrate. Nanowires can be grown by selectively filling the channels above a metal strip, as represented by the channels on the right end.

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filling the pores of the PAA template, arrays of aligned nanowires uniform in diameter and length, are obtained reproducibly and economically.[11] However, PAA has some severe disadvantages that preclude the development of devices using this type of nanowire array: PAA is a brittle ceramic film grown on soft aluminum metal. Great care needs to be exercised in the preparation of the aluminum substrate and in the manipulation of the anodic film, as defect-free PAA films are required in order to achieve uniform filling of the pores with the nanowire material. Moreover, between the porous layer and the aluminum substrate, there is a continuous and dense alumina barrier layer that prevents the direct physical and electrical contact between the pore (or the nanowire) and the substrate (Fig. 1a). To reach the pores from the barrier-layer side, the most common practice is to etch away the aluminum substrate and subsequently to etch away the exposed barrier layer, thus opening up the blocked ends of the alumina channels. This process, however, leaves an unsupported PAA film that is fragile and unsuitable for device fabrication. It is therefore of great interest to develop methods to grow PAA films on rigid substrates of technological relevance and to establish contacts to *both* ends of the pores (or of the nanowires) while the PAA is still attached to the substrate, as depicted in Figure 1d. Such a technology would allow one to integrate addressable arrays of parallel nanowires as active components in electronic, thermoelectric, optical, field emission, and sensing devices.

Crouse et al. have demonstrated that PAA films up to 2 μm thick can be grown by anodizing an aluminum film deposited on a silicon wafer.[12] They found that the barrier layer between the porous film and the silicon wafer had an inverted morphology with voids between the barrier layer and the wafer, as depicted in Figure 1c. A similar morphology was observed in PAA grown on indium tin oxide (ITO)-coated glass.[13,14] Other structures consisting of PAA films on silicon wafers have been reported to date,[15–20] yet all possess two important features that make them unattractive for nanowire array fabrication: the low length-to-diameter aspect ratio (~20–50) of the channels, which extend only up to 2 μm in length, and the presence of the insulating barrier layer between the pores and the substrate. In some of these reports, electrochemical deposition in the channels was achieved following an isotropic alumina etch step or following the formation of tiny conduction paths across the barrier layer.

In this paper, we report a procedure to fabricate large-area arrays of high-aspect ratio nanowires in PAA films on silicon wafers, electrically connected to the substrate (as in Fig. 1d). Furthermore, we demonstrate the use of these structures in the characterization of the transport properties of the nanowires.

2. Results

Porous anodic alumina films were grown on n-type silicon wafers, as reported by Crouse et al.,[12] by the double anodization process.[21] Aluminum was deposited on the silicon wafers in a modified thermal evaporator. The 4 in. (1 in. = 2.54 cm) silicon wafers were placed in close proximity to the Al source (15 cm above the source) to obtain a thick layer of deposited aluminum, compromising the thickness uniformity across the wafer. The aluminum film thickness varied from 12 μm at the center to 6 μm at the edges of the wafer. The total thickness could be further increased by depositing multiple Al layers on top of each other. The samples were electrochemically polished before anodization. The first anodization was carried out for 10 min, corresponding to the formation of about 1 μm of alumina. This layer of alumina was etched away and the sample was re-anodized under the same conditions until the aluminum was fully anodized. Continuous porous anodic alumina films with a good degree of pore ordering (as in Fig. 1b) and high optical transparency were obtained by this method. However, if the thickness of the aluminum layer was greater than ~1 μm, the alumina layer became separated from the underlying wafer once the anodization was completed. Even if the anodization was performed on a selected area of the Al film, patterned by an insulating coating, the alumina film on the fully anodized area still became detached from the substrate and curved away from it, being held to the wafer only by the protected aluminum metal around it. It is evident that the volume expansion during the conversion of aluminum to PAA leads to the appearance of compressive forces within the film, which are relaxed by the separation from the substrate. This is a surprisingly straightforward method for obtaining free-standing PAA films, which avoids the use of chemicals for etching away the aluminum.

Figure 2 shows scanning electron microscopy (SEM) and atomic force microscopy (AFM) images of the two faces of the PAA film after its spontaneous detachment from the silicon wafer at the completion of the anodization. The images show that the porous structure of the PAA film extends from one face of the film to the other. The solution-facing side displays well-defined pore openings, but also a rough surface that results from the indentations on the surface at the end of the first anodization step[21] and from the etching action of the solution. The substrate-facing side, however, is characterized by a flat

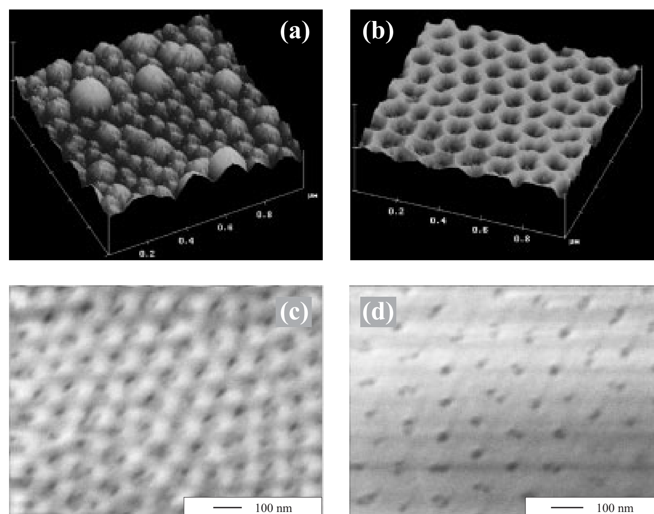

Fig. 2. AFM images of the surfaces of a PAA film that detached from the silicon substrate on which it was anodized [a) electrolyte-facing, top surface; b) wafer-facing, bottom surface], and SEM images of the same surfaces [c) top surface; d) bottom surface].

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surface (mirroring the flatness of the silicon wafer), interrupted by the pore openings. The SEM image shows that the pore openings are not very well defined, suggesting the presence of an inverted barrier layer near the pore ends. However, the extreme flatness of this surface, compared with the surfaces of PAA films formed on Al films, and the ease of detachment make the free-standing PAA films thus obtained very attractive as contact masks for nanoscale pattern-transfer processes.[22–27]

In order to prevent the detachment of the anodic alumina film, we explored the use of adhesion layers between the aluminum layer and the substrate. Thermal-oxide-coated wafers were found to be appropriate substrates for the growth of PAA films. No detachment of the PAA film from the wafer was observed upon completion of the anodization. Instead, the completion of the anodization was manifested by a sharp current decrease and a color change. In this case, the barrier layer is not inverted, but rather it is thick and continuous (see Fig. 3). It should be mentioned that due to the insulating nature of the silicon oxide layer, nanometer-sized aluminum particles (indicated by arrows in Fig. 3) were occasionally observed trapped between the alumina barrier layer and the silicon oxide layer, particularly beneath pores with a smaller-than-average diameter.

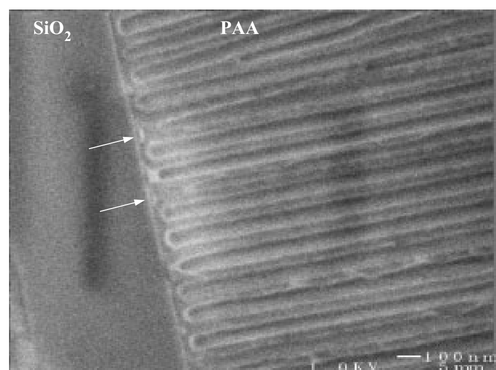

Fig. 3. SEM image of the interface between the PAA film and the silicon oxide layer after an anodization on a SiO_2-coated silicon wafer. The arrows point to trapped aluminum particles.

The formation of large trapped islands of unanodized material was prevented by the gradual variation in Al film thickness across the sample. Similar results were obtained when we used glass slides coated with 20 nm of titanium as a substrate, although the structure was not as robust, and alumina flakes detached if the sample was rubbed or cut. The PAA–glass structures, however, have the advantage of being transparent to visible light.

We further explored the possibility of growing the PAA films on substrates with conducting adhesion layers. Such a substrate could then be used to direct the selective etching of the barrier layer, to grow nanowires in the pores, and to make electrical contacts to the nanowires on one end (Fig. 1d). Care was taken in choosing the composition of the substrate, considering that many conductors will react under the anodization conditions that produce PAA, resulting in anodic dissolution and/or gas formation. Furthermore, in some cases insulation was applied to the edges of the sample to prevent contact between the electrolyte and the layers underneath the aluminum film during anodization. PAA films were grown on platinum-coated silicon wafers, with a titanium film (40 nm thick) serving as an adhesion layer between the Pt layer (50 nm thick) and the thermally oxidized wafer. The anodization current reached a steady-state value within minutes, as is typically seen in PAA-forming constant-voltage aluminum film anodization, and then the current increased sharply as the aluminum was fully consumed throughout the thickness of the layer at its thinnest zone. The current rise is due to the electrolysis of the acid at the surface of the platinum film. The current flow was stopped at this point, since gas bubbles would have broken through the PAA, leaving behind circular areas of exposed substrate. Alternatively, the thickness of the aluminum was intentionally graded along one dimension of the sample. As the anodization in the thinner areas reached completion and the current surged, the sample was gradually pulled out of the electrolyte bath until a new steady-state current was re-established and thicker areas continued to be anodized.

At the interface between the platinum and the alumina layers, SEM imaging revealed the presence of a barrier layer. However, this barrier layer was not continuous: a fraction of the pores reached the metallic layer through holes in the barrier layer. As a result, we could grow metallic nanowires in the areas that were fully anodized. Figure 4a shows an SEM image of the cross-section of a PAA membrane on a Pt-coated wafer in which some channels have been filled with bismuth nanowires by electrochemical deposition. The aspect ratio of these nanowires, 60–70 nm in diameter, is very high, exceeding 100. Aspect ratios exceeding 300 were achieved for thinner nanowires, 30 nm in diameter. The image in Figure 4a was taken at the interface between a fully anodized region and a region in

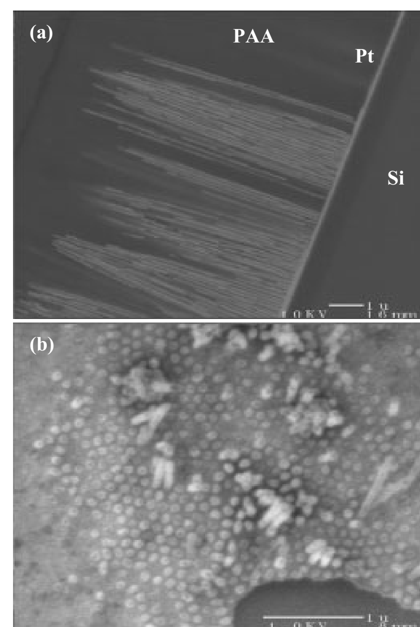

Fig. 4. a) Cross-section SEM image (backscattering mode) of bismuth nanowire arrays grown on a Pt-coated silicon wafer. b) Top view of gold nanowires grown on a Pt-coated silicon substrate after dissolution of the PAA template.

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which the PAA pores have not yet reached the Pt surface. The Figure shows dense groups of continuous nanowires growing from the Pt layer toward the solution side of the PAA template. The density of the nanowires decreases sharply toward the top of the image, as we approach the region where the aluminum was not yet fully anodized. There is also a large distribution of nanowire lengths within the groups of nanowires, indicating that the openings at the barrier layer are not of uniform size and quality. This property was actually found to be advantageous in the electrical characterization of the nanowires, as will be described later. Figure 4b shows an SEM image of a gold nanowire array obtained by the electrochemical deposition of gold into the channels of a PAA template on a Pt-coated wafer. The image shows the Pt surface after the complete etching of the PAA membrane, which exposes the nanowires. In this image we see a region of short nanowires that did not shift from their original positions, nor lose their orientation, retaining the hexagonal arrangement of the pores of the template.[28] Energy-dispersive spectroscopy (EDS) analysis indicated that the nanowires were made of gold while the surrounding surface was made of Pt. Since the nanowires are the inverted image of their template, this finding clearly indicates that the interface between the PAA and the Pt consists of non-interconnected pore openings.

To achieve a higher uniformity in the structure of the template and in the nanowire filling within a large area, a different conducting layer was employed. By coating the silicon wafer with a 250 nm thick titanium film before Al deposition, a dramatic change in the anodization characteristics was observed. During the constant-voltage anodization of the aluminum film, the current reached its steady-state value within several minutes. As areas were depleted of aluminum and the electrolyte reached the titanium layer in these areas, the current decreased significantly, and the color of these areas turned from metallic gray to dark purple. A new steady-state current value was established after the aluminum was consumed over the entire wafer area. Due to variations in the PAA film thickness, resulting from the non-uniform thickness of the evaporated aluminum film, interference patterns along the thickness gradient were visible in the anodized samples. The titanium layer served as an auxiliary conducting layer once the aluminum was oxidized. It served also as an adhesion layer, preventing the separation of the PAA film from the wafer. The titanium layer was oxidized under the operating conditions for Al anodization, forming a porous oxide coating. However, a low-resistance metallic titanium layer remained underneath this oxide.[29] The PAA barrier layer over the titania had the inverted morphology. The titanium was used to induce an electrochemical process at the interface between the substrate and the PAA for the purpose of removing the barrier layer. The process consisted of immersing the sample in a potassium chloride electrolyte and cathodically polarizing the titanium layer for several minutes at –2.25 V versus a platinum plate electrode. Under these conditions, hydroxide ions were produced at the surface of the titanium, locally increasing the pH. Since dissolution of the PAA membrane is enhanced at > pH 8,[30] the process led to the thinning of the alumina. Figure 5 shows a cross-sectional view of

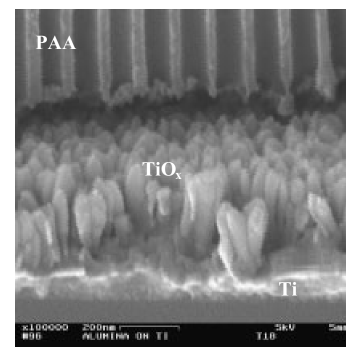

Fig. 5. Cross-section SEM image of the interface between the PAA film and the titanium/titanium-oxide layer after an anodization on a Ti-coated silicon wafer. The sample was then subjected to the pore widening and the electrochemical barrier layer removal processes described in the text. From top down we observed the ordered alumina channels, oxidized titanium pillars, and a titanium film coating the silicon surface.

the PAA on a Ti-coated wafer after barrier layer dissolution. One notices that most channels lack a barrier layer, ending in a partially or completely open pore. Hints of the inverted barrier layer can be seen in some of the channel ends. When the cathodic polarization was applied to a Pt-coated substrate, it resulted in a current density higher by an order of magnitude and defects soon became visible in the film. A cross-sectional SEM inspection (Fig. 6) revealed that these defects were localized at the substrate–PAA interface as cave-like structures, while the solution–PAA interface remained flat and undamaged. These

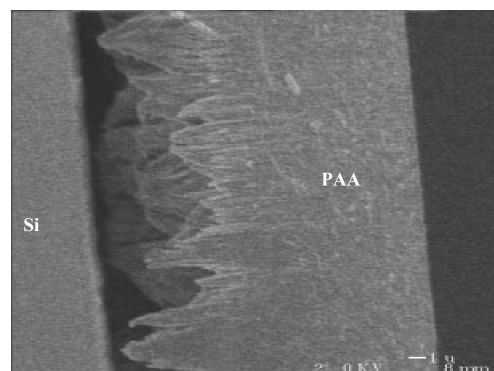

Fig. 6. Cross-section SEM image of the PAA and the wafer (on the left) after an anodization on a Pt-coated silicon wafer. The sample was subjected to the electrochemical barrier layer removal process for a prolonged period of time. The process caused damage in the form of gaps in the PAA structure starting at the interface with the substrate and extending up to ~5 μm into the PAA layer. The undamaged, external surface of the PAA is seen on the right.

observations imply that localized electrochemical reactions at the substrate–electrolyte interface lead to the selective etching of the barrier layer without the disruption of the porous alumina structure.

The barrier layer-depleted, silicon-wafer-supported PAA templates were used as substrates for electrochemical deposition of metals and low bandgap semiconductors to produce nanowire arrays. Figure 7 shows a cross-section of such a template after being overfilled with bismuth telluride. In contrast with the Pt-coated samples in which the density of nanowires varied significantly across the sample, here the growth of the nanowires was uniform over the entire area of the sample

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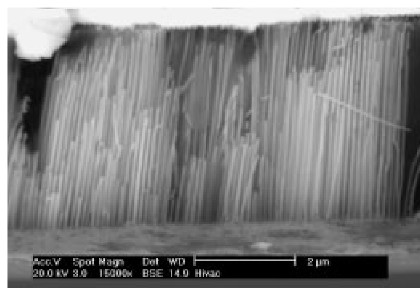
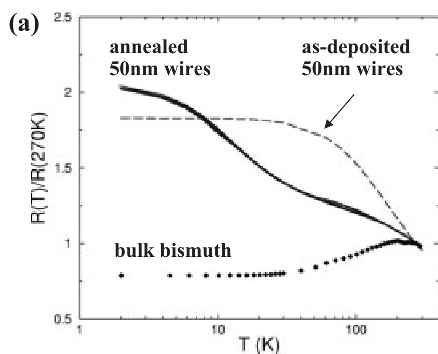


Fig. 7. Cross-section SEM image of bismuth telluride nanowires grown in a barrier-layer-depleted PAA template on a Ti-coated wafer.

(~ 1.5 cm^2). Pore widening was applied before the deposition to tune the diameter of the channels.

Due to the rigidity of the substrate, the nanowire-filled samples can be manipulated considerably without the danger of cracking, a common problem encountered when processing conventional PAA films (free standing or on aluminum sheets). Thus, we were able to use these assemblies to perform measurements to characterize the nanowire arrays. For electrical measurements, we made use of the underlying conducting layer to make electrical contact with the bottom of the nanowire array (Fig. 1d). A second electrical contact was made with the exposed ends of the nanowires at the top surface of the sample by attaching a gold wire, either to the electrodeposited material that overflows from the pores or to a patterned metallic layer deposited on top of the PAA layer. Figure 8 shows the temperature dependence of the resistance of a 50 nm-diameter bismuth nanowire array, grown on a Pt-coated substrate. The resistance characteristics are very similar to those reported previously[31,32] for 200 nm-diameter polycrystalline bismuth nanowire arrays. We also took advantage of the relatively low nanowire density and the high dispersion in the nanowire length in arrays grown on Pt-coated wafers to sample the electrical properties of a small number of nanowires, even possibly an individual nanowire. This was achieved by electron-beam (e-beam) deposition of a patterned 100 nm thick gold film on top of the PAA layer prior to the electrodeposition of the nanowires. As long as the deposited layer thickness was not greater than twice the pore diameter, the pore openings remained unplugged, allowing electrolyte penetration into the PAA channels. This top gold film was used during the electrodeposition process to detect the emergence of the first nanowire(s) from the template, by monitoring the voltage between this film and the cathode.[33] A voltage short triggered the termination of the deposition. The small deposition area and the inhomogeneity of the interface between the Pt and the PAA film, which causes the nanowires to grow at different rates, helped ensure that only a small number of nanowires reached the top surface and shorted the two metallic films. Measurements carried out on arrays report average values for quantities which are affected by inhomogeneous broadening due to geometrical and structural variations from wire to wire. Samples prepared by this method probe a small number of wires and are being used to determine the importance and the extent of such wire-to-wire variations.[34]



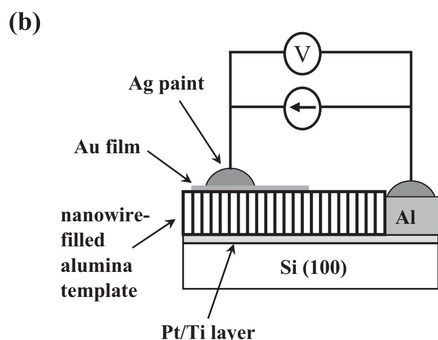


Fig. 8. a) Resistance versus temperature characteristics of electrodeposited 50 nm diameter bismuth nanowire arrays normalized to its value at 270 K and compared to the normalized resistance for electrodeposited bulk bismuth. b) Scheme of measurement set-up.

As another example of the versatility of PAA films prepared by the method reported here, we present a new method for patterning PAA. Previously, the patterning of PAA films was achieved by etching regions of the anodic alumina film after anodization (using a pattern transfer layer).[35] For PAA films on silicon wafers, in addition to this post-anodization selective-etch method, patterned PAA films were obtained by employing a patterned substrate. On a Ti-coated silicon substrate, an array of lines of silicon oxide was deposited by sputtering. The trenches between the lines were 2.5 mm long, 10–250 μm wide, and 500 nm deep. Aluminum was evaporated on the patterned substrate, electrochemically polished, and anodized. Since the entire substrate was originally coated with a continuous conducting layer of titanium, the patterned aluminum and PAA structures did not need to be continuous. Figure 9 shows PAA lines obtained by this patterning method in the trenches between slabs of silicon oxide. Detailed examination of the cross-section of the structures shows that due to the poor step coverage of the aluminum deposition, weak links were formed between the sections of the aluminum film in the trenches and those on top of the silicon oxide structures (Fig. 9b). During the subsequent anodizations and etchings, the connecting necks were broken or dissolved, leaving PAA structures mostly within the trenches (compare Figs. 9b,c). Since the side walls of the aluminum lines were exposed to the electrolyte, pores grew simultaneously, vertically from the top surface down and horizontally from the side walls inward. Thus, only pores within a region along the center of the PAA lines actually reached the substrate (Fig. 9e). A barrier layer grew diagonally along the top angle bisectors, where pores from the top and from the side surfaces met (Fig. 9f).

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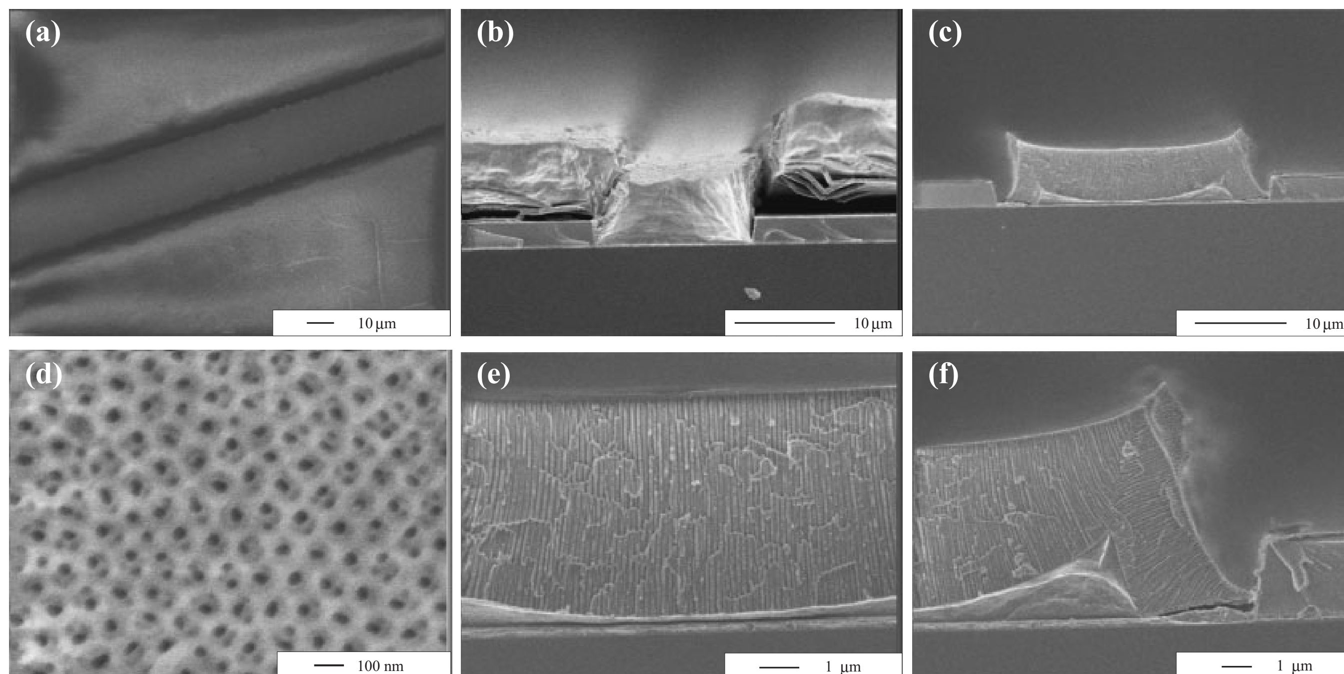

Fig. 9. Patterned lines of PAA on a Ti-coated, SiO_2-patterned wafer [a) top view of a PAA line between two slabs of SiO_2; b) side view before anodization; c) side view after anodization; d) high magnification of top view of the PAA line shown in (a); e,f) high-magnification cross-sectional view of the PAA line shown in (c)].

3. Discussion

We have reported a novel process for the fabrication of porous anodic alumina membranes and arrays of nanowires embedded in alumina templates on the surface of a silicon wafer substrate (our preliminary work on glass shows that other rigid substrates can also be used). A schematic representation of the process is depicted in Figure 10. The rigid substrate is coated with thin layers of material, which can have one of the following purposes: a) adhesion layers that prevent the separation of the PAA films from the substrate due to the strain generated during the expansion of aluminum into anodic alumina; b) conductive layers that serve to induce electrochemical reactions at the PAA–substrate interface, leading to either etching or deposition; c) patterning layers that define areas of porous anodic alumina formation and nanowire growth. The designed substrate is placed in a thermal evaporator, and a thick layer of several microns of aluminum is deposited. A quick electrochemical polish step is used to remove the minor surface roughness that results from the preferential growth of the aluminum grains into triangular-shaped terraces during the thermal deposition. The thickness of the aluminum layer was reduced by only several tens of nanometers during this process. The polished aluminum layer is anodized, taking into consideration the desired values for the different geometrical parameters of the porous film (such as pore diameter and channel length) and the importance of pore ordering. On areas where a conducting layer was deposited on the wafer and an inverted barrier layer of relatively low thickness was formed, an electrochemical process can be used to selectively etch the barrier layer and open the channels at the interface with the substrate. Deposition techniques are then employed to fill the pores of the PAA film with nanowires, and further patterning is possible by etching out sections of the PAA film.

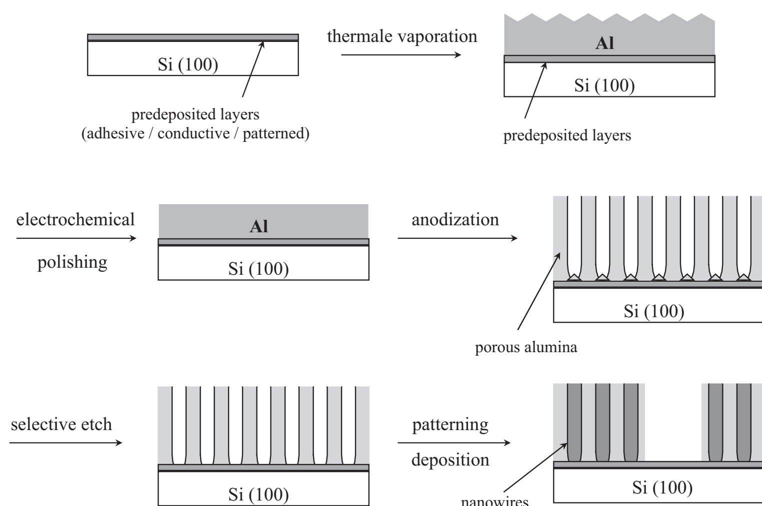

Fig. 10. Schematic representation of the fabrication of PAA films and nanowire arrays on silicon wafers and other solid substrates.

Our studies show that the substrate strongly influences the structure of the barrier layer at the PAA–substrate interface. The anodic behavior of the inter-

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face layer determines whether the PAA channels will be closed by a barrier layer at the PAA–substrate interface, whether they will be open locally, or whether they could be opened uniformly. Particular attention has been given to the case of titanium as a conducting and adhesion layer. Our study shows that the aluminum–titanium bilayer has quite unusual anodization properties. At constant anodization voltage, as the anodization front passes from the aluminum layer to the titanium layer, the current decreases to less than 1 % of its steady-state aluminum anodization value. The anodized titanium serves as an anodization barrier, yet the anodic titania shows significant porosity. The underlying metallic titanium remains conductive, and electrochemical reactions can occur through the oxide layer. On the silicon wafers, the alumina barrier layer at the alumina–titania interface is inverted and is substantially thinner compared to the barrier layer obtained at the alumina–aluminum interface under the same experimental conditions. The structure of the titania barrier layer has not yet been investigated in detail, and reactivity of the titanium toward the silicon substrate under the process conditions cannot be strictly excluded. Nevertheless, Ti-coated silicon wafers proved to be well-suited substrates for templated nanowire-array fabrication by electrochemical deposition in PAA templates. Other conducting films tested by us (e.g., Cu, Pd–Au, Ag, Pt) gave rise to complications due to their anodic behavior (breakdown or dissolution) or showed poor adhesion to the substrate. However, other so-called "valve metals" (e.g., Zr, Nb, Hf, Ta)[36] may give results similar to titanium.

We believe that the reported process has a strong impact on the prospect of developing PAA-based and nanowire-based functional structures. First, the fabrication process has been simplified, reducing the number of necessary polishing and etching steps. Second, the structure is directly made on the surface of the technology-relevant substrate, and therefore, no transfer, alignment or bonding steps are necessary. The PAA structure is fundamentally integrated into the surrounding device structure by design. Third, the rigidity of the substrate protects the fragile PAA film from mechanical damage, substantially extending the range of conditions that the film is able to withstand. Thus, the silicon substrate-supported PAA film is compatible with many processes that would otherwise damage the free-standing or aluminum-supported PAA film. This, in effect, translates into faster and cheaper processing of substantially larger samples. Fourth, since the barrier layer removal process is not dependent on the thickness of the alumina film, the deposition of nanowires with high aspect ratios (typically ~ 10^2) is feasible.

We have demonstrated that the adhesion between the PAA layer and the substrate can be controlled to the full extent. The process, therefore, can also be harnessed to prepare optically transparent free-standing PAA films, with a good control over their surface roughness and their surface topography.

The process described here also offers a means for the fabrication of several new "flavors" of arrays of nanowires in PAA templates that were impossible or difficult to prepare with the previously available technology. Primarily, the location of the growth of nanowires can be prescribed by the design of the substrate, particularly by the patterning of conducting and insulating regions on the substrate. Furthermore, the patterns can be designed so that areas on the wafer can be biased independently (Fig. 1d). This design will allow the fabrication of several arrays of nanowires in a single PAA film,[37] each array being distinct in terms of its composition (or its composition profile along the main nanowire axis[38]). Such a "super-array" is well suited for sensing applications of nanowires. In addition, this process offers a means of generating nanowires of different lengths within the same template, dictated either by the topography of a patterned substrate or by the thickness profile of the deposited aluminum film, and possibly by planarization steps. Lastly, as seen in Figure 9, non-planar PAA films can be designed and prepared, in which the orientation of the channels (or of the nanowires) changes continuously (as in curved films) or abruptly (as in films with kinks). We found, however, that some formations are not easily achieved due to factors like internal strain in the growing film, and the geometric dependence of the pore density on curvature and film thickness. Non-planar porous anodic alumina structures are an exciting subject for further exploration.

4. Conclusions

We have developed a method for the incorporation of porous anodic alumina films and the templated growth of arrays of nanowires on the surface of rigid substrates, in particular silicon wafers, by the direct anodization of aluminum on the desired substrate. Poor adhesion between thick porous anodic alumina films and the substrate was recognized and resolved by interfacial layers. By applying metallic coatings on the substrate, we controlled and modified the structure of the barrier layer and guided the electrochemical growth of nanowires within the channels of PAA without detaching the anodic film from the supporting substrate. Unlike free-standing PAA films, the resulting structure is robust enough to be grown on large areas and manipulated in a variety of ways. We demonstrated the convenience of the technology by the growth of patterned PAA on a non-planar substrate and by the use of the obtained assembly for the investigation of the electrical transport properties of the nanowires. We envision the implementation of this technology in the fabrication of nanowire-array-based devices.

5. Experimental

Thick aluminum films were obtained by thermal evaporation of Al (Plasmaterials, 99.999 %) on 4 in. (~ 2.5 cm) n-type silicon substrates (Wafernet, 1–10 Ω cm) in a custom-built chamber (base pressure: 10^{-6} Torr; source–target separation: 15 cm; average deposition rate: 40 nm s^{-1}). Ti films were obtained by sputtering (Applied Materials Endura System). SiO_2 layers were obtained by sputtering or by wet thermal oxidation in a tube furnace (MRL Industries Model 718). Au films and Ti/Pt bilayers were obtained by e-beam evaporation (Temescal Semiconductor Products).

Electrochemical polishing of the Al films was carried out in a H_3PO_4(95 vol.-%): H_2SO_4(5 vol.-%):CrO_3(20 g L^{-1}) solution at 85 °C and 20 V. The anodizations were carried out in a 4 wt.-% oxalic acid solution at 18 °C and 50 V for pores ~ 60 nm in diameter, in a 0.04 M oxalic acid solution at 4 °C and 85 V for pores ~ 85 nm in diameter, or in a 20 vol.-% sulfuric acid solution at 0 °C and 20 V for

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pores ~30 nm in diameter. In both processes, a Pt sheet was used as a counter electrode. The back surface and the edges of the sample were insulated by an SiO_2 coating, a wax coating (CrystalBond 509, Buehler), or a nail-lacquer coating. The resulting alumina film was etched away in a H_3PO_4(3.5 vol.-%): CrO_3(45 g L^{-1}) solution for 16 h, and the remaining aluminum was re-anodized under the same conditions until the metal film was fully oxidized. To adjust the pore diameter, the alumina film was dipped in 5 vol.-% H_3PO_4 or in 20 vol.-% H_2SO_4. The barrier layer was electrochemically etched from PAA layers anodized at 50 V on Ti-coated wafers by subjecting the Ti interface layer to a cathodic bias of 2.25 V in a dilute KCl aqueous solution for 15–30 min. Nanowires were electrodeposited from aqueous solutions in a 3-electrode set-up under constant potential vs. a saturated calomel electrode.

Scanning electron microscopy (SEM) (JEOL 6320FV) and atomic force microscopy (AFM) (Digital Instruments Nanoscope IIIa, tapping mode) were employed for the structural analysis of the alumina films. Electrical resistance measurements were carried out in the chamber of an automated DC Magnetic Property Measurement System (Quantum Design) in a 2-point *V*–vs.–*I* measurement geometry.

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