Alternative Front-End Electronics (for LBNE & PET)

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LAPPD Collaboration Review
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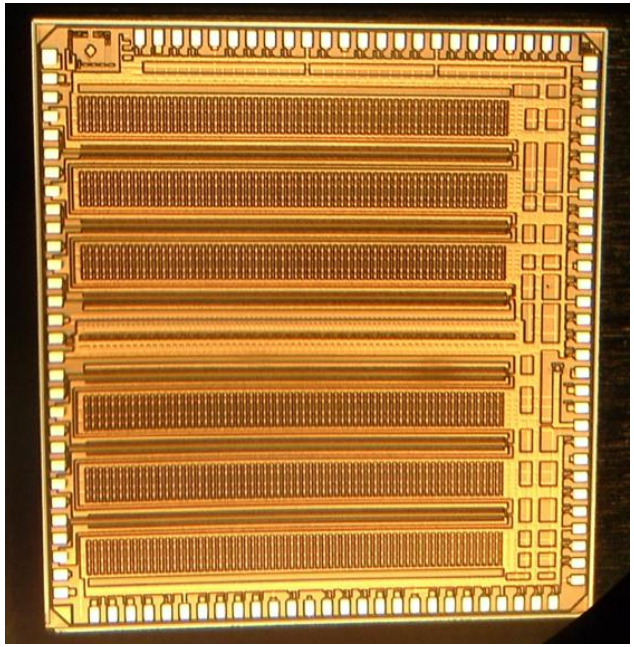
Why consider alternative ASICs?

- PSEC-4 has demonstrated:
  - 6 channels, 256 samples each
  - Excellent bandwidth (> 1.5 GHz)
  - Fast sampling rates (> 10 GSa/s)
  - Event rate (~100s of kHz)
  - Low noise (< 1 mV_{RMS})



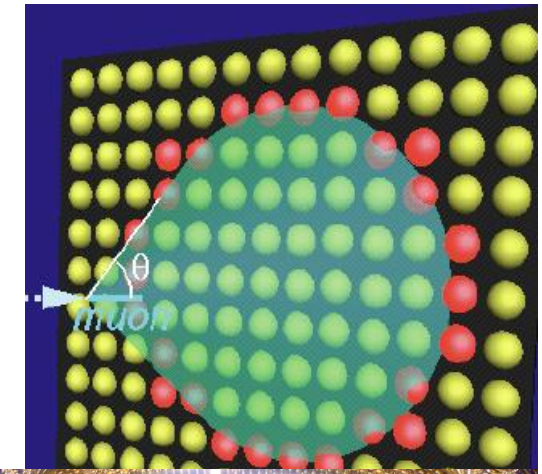
- Not all applications need/want fast sampling rate or high bandwidth as highest priority.
  - Will focus primarily on buffer depth (~trigger latency) and continuous operation / multi-hit buffering (low dead-time).

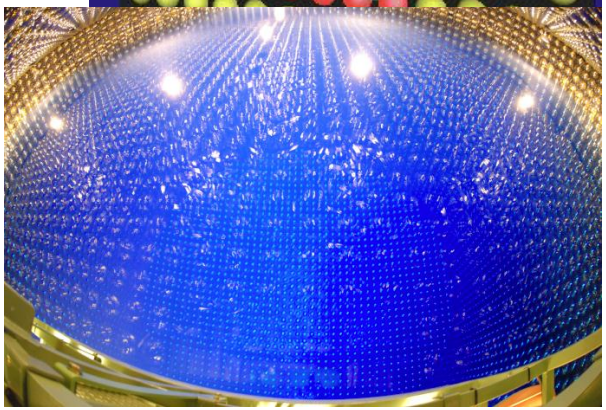
Apologies in advance

- Most of my experience is related to collider experiments…

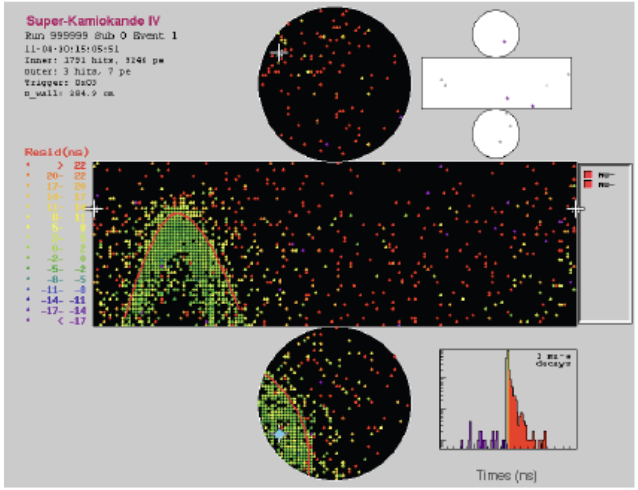
- My knowledge of electronics requirements for LBNE and PET is largely from the last few days.

Neutrino Experiments

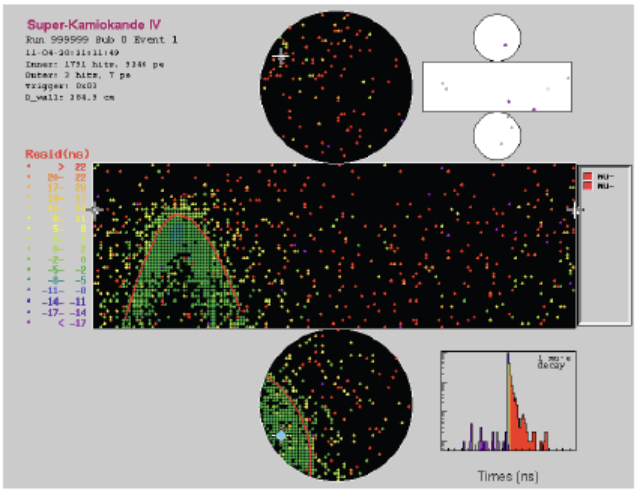




Normal



Fast

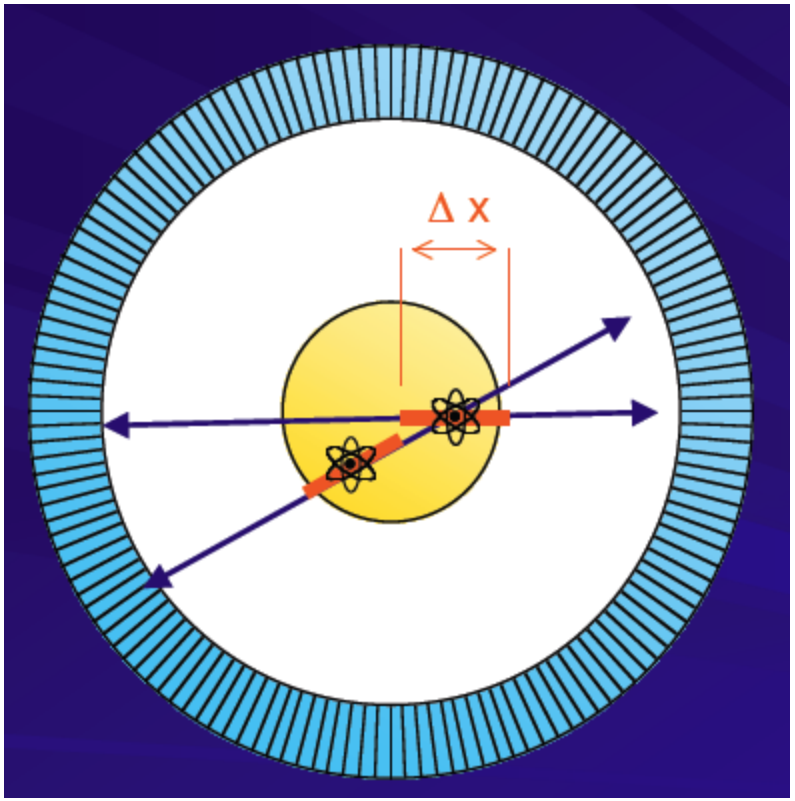


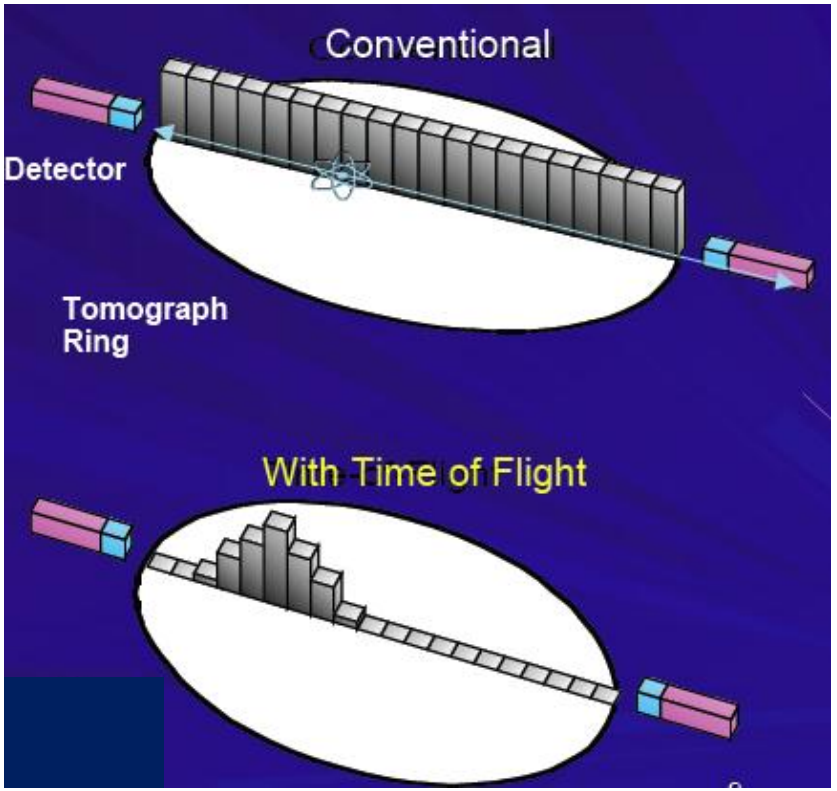
- Other detectors (e.g., SK) do well w/ σ_t ~ns.
- LAPPD MCPs could do much better timing… but what is actually needed?

- Trigger requirements for front-end: ideally system is "triggerless" – ***all*** hits collected and sent to computing farm for event building.
- Low dead time, multi-hit buffering to collect all hits.

*Pictures from Kate Scholberg's talk at April fast timing workshop

Positron Emission Tomography



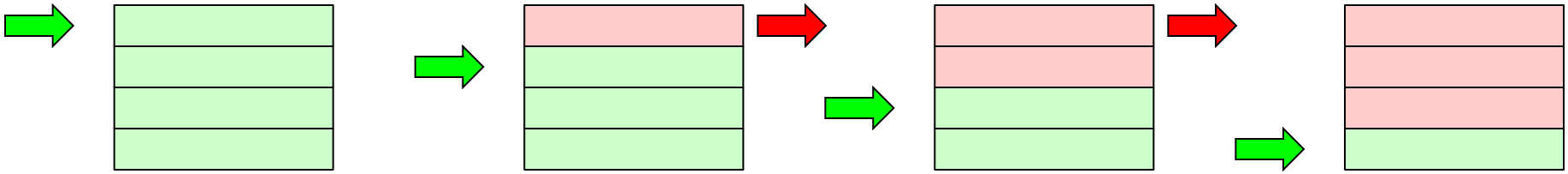


- Time-of-flight PET benefits from good timing resolution (scintillators limit this to σ_t~100 ps).
- High rate (~MHz), requires low dead time.

*Pictures from Patrick Le Du's talk in PSEC doc library

Multi buffering

"Multi-buffering" can reduce dead time for Poisson-distributed events



Event is stored in first buffer

Event occurring during readout of first event is stored in second buffer

R: event rate [Hz]
T: readout time [s]
LT: "live time"
N: Number of buffers

Cumulative distribution function for Poisson-distributed events:

$$LT = e^{-R \cdot T} \sum_{i=0}^{N-1} \frac{(R \cdot T)^i}{i!}$$

R = 1 kHz, T=400 μs

N	LT
1	67 %
2	94 %
3	99.2 %
4	99.9 %

Alternative ASICs…

More apologies…

- And all of my “hands-on” ASIC experience is using those developed in Hawaii…

- Will try to cover at least a few other ASICs as well.

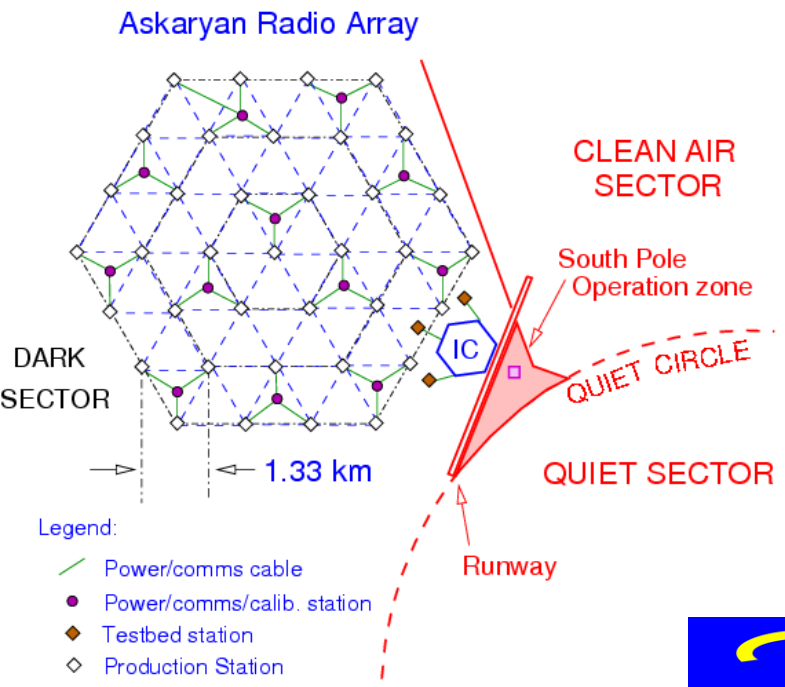
Snapshot of fabricated ASICs (Hawaii)

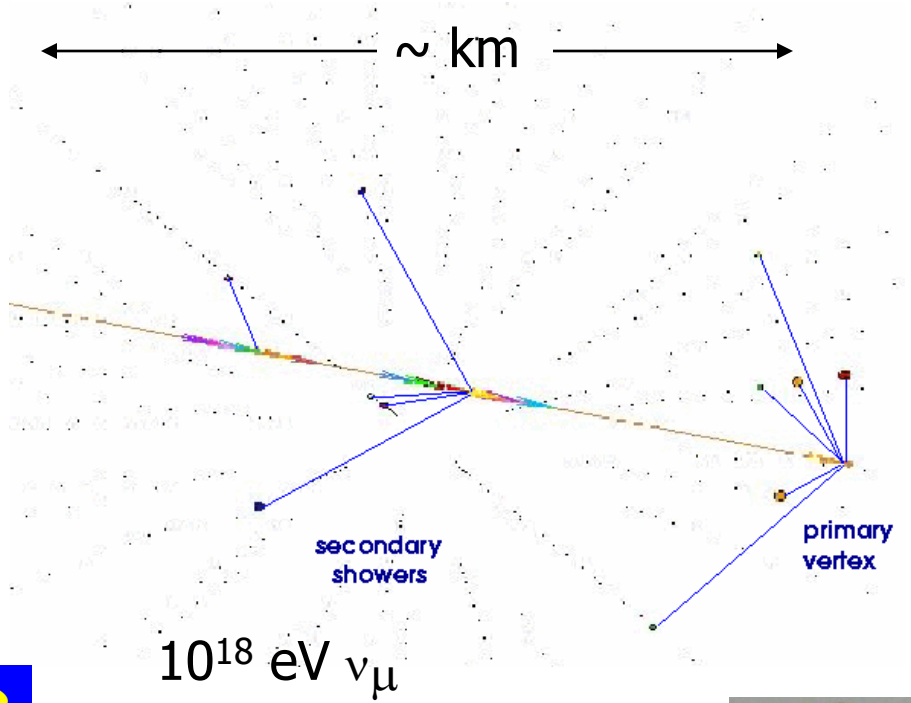
All in TSMC 0.25um

ASIC	# Ch.	Sampling (GSa/s)	ABW (GHz)	# Samples	# Store cells/chan.	Remarks
LAB3	8+1	0.5-3.2	0.8	256+4	same	
BLAB1	1	0.5-6	0.2	64K	same	
BLAB2	16	0.5-4	0.2	3k	same	- Amplification
BLAB3,3A	8	0.5-4	0.3	2*64	32K	- 2stage x-fer - Amplification
IRS, IRS2 ➔ IRS3	8	0.5-3.3	~1	2*64	32K	- 2stage x-fer
TARGET	16	0.5-2.5	0.2	4K	same	
TARGET2,3 ➔ TARGET4	16	0.5-2.0	0.4/1	2*32	16K	- 2stage x-fer - Amplification on TARGET2
STURM	8	10-20	~2	4*8	same	
STURM2	8+1	1-200	~3	4*8	same	
LARC	64	0.5-3.5	0.5	1K	same	

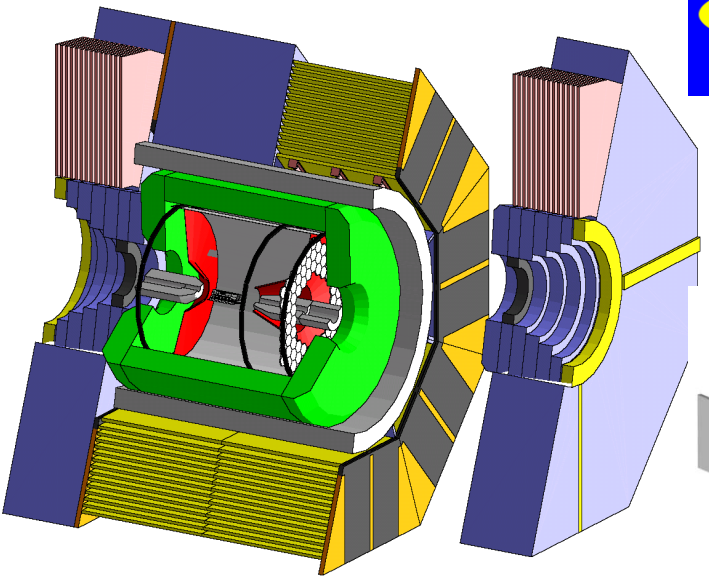
➔ Variety of bandwidths, depths, other features.

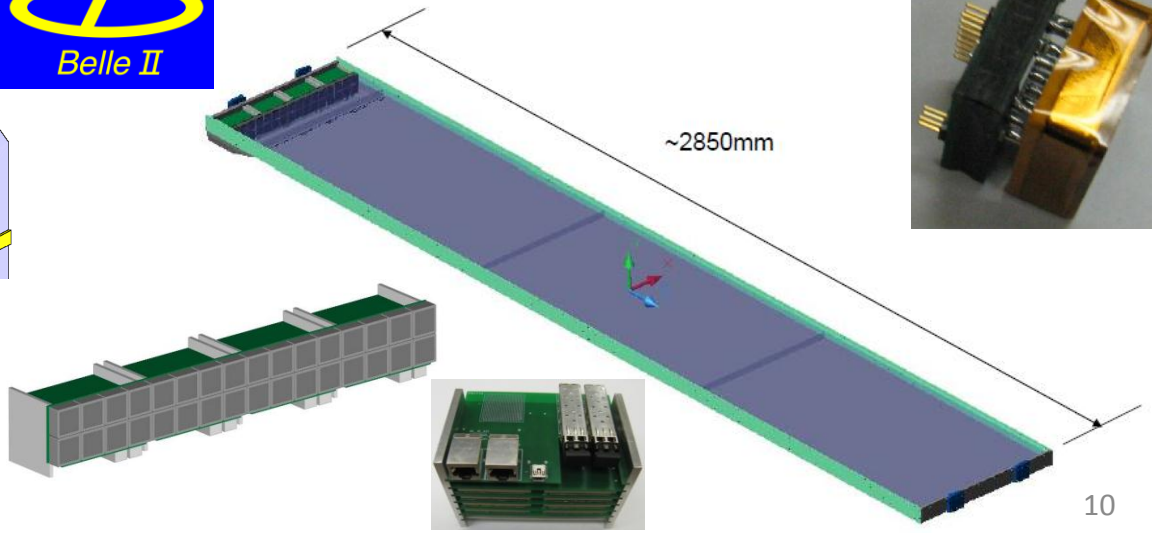
Deep sampling for other applications…



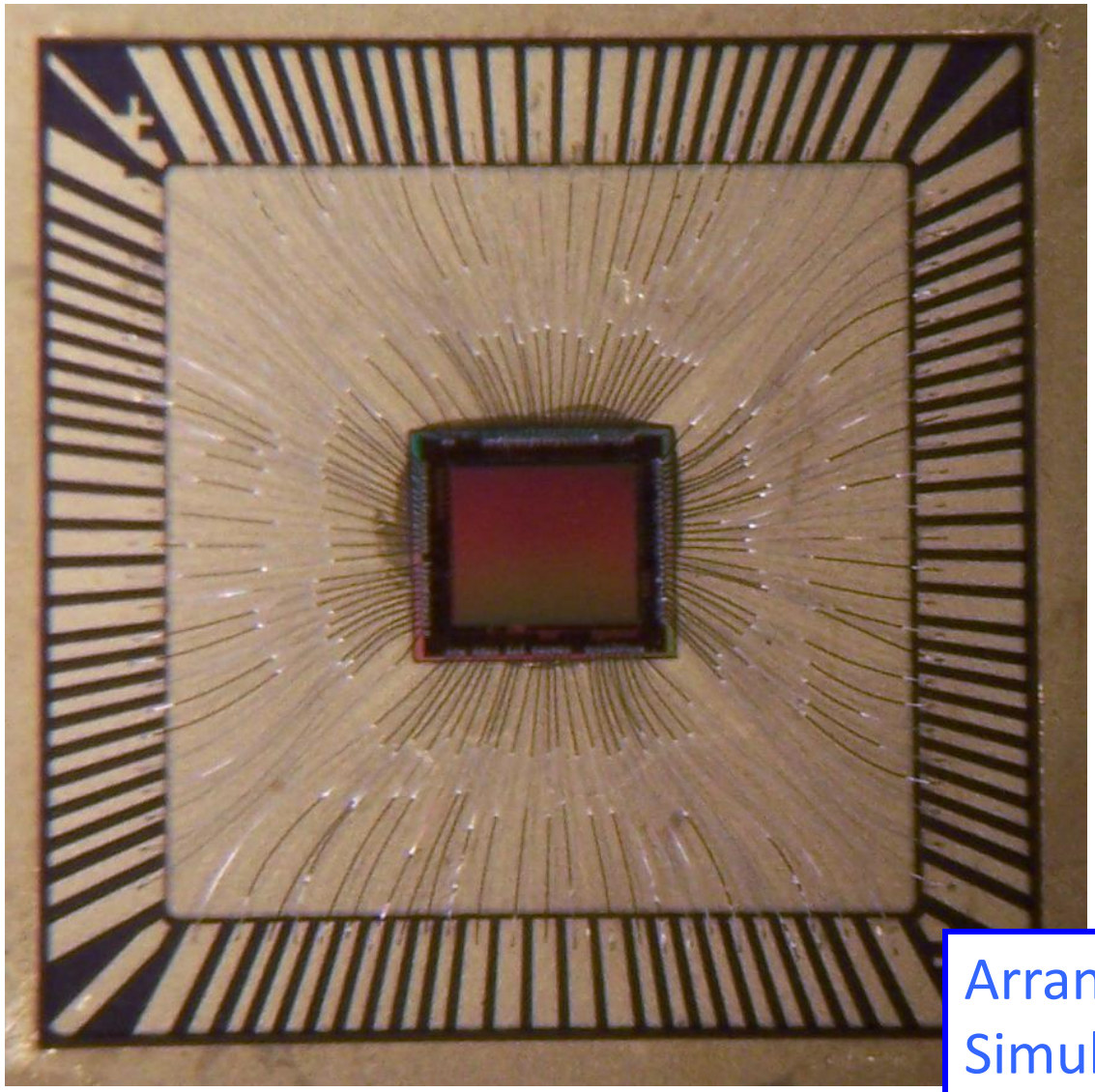


10^{18} eV ν_μ





Deeper storage: Buffered LABRADOR (BLAB1) ASIC



3mm x 2.8mm, TSMC 0.25um

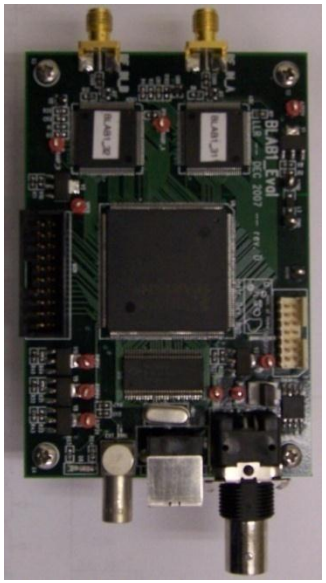
- Single channel
- 64k samples deep, same SCA technique as LAB, no ripple pointer
- Multi-MSa/s to Multi-GSa/s
- 12-64us to form Global trigger

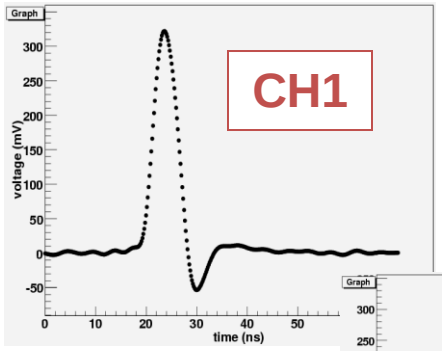
Arranged as 128 x 512 samples
Simultaneous Write/Read

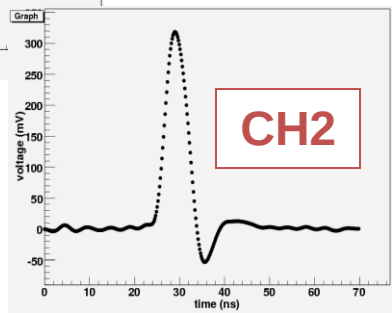
BLAB1 High speed Waveform sampling

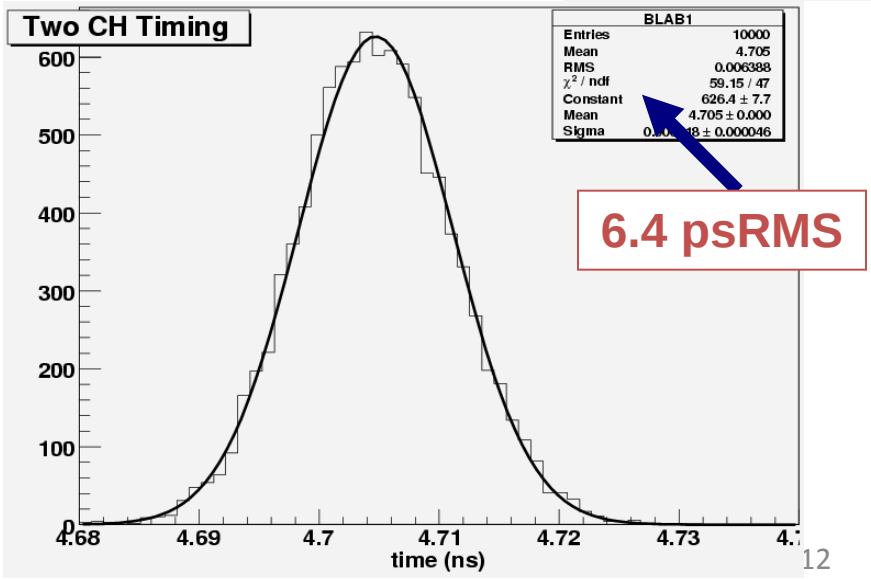
- Comparable performance to best CFD + HPTDC
- MUCH lower power, no need for huge cable plant!
- Using full samples reduces the impact of noise
- Photodetector limited

NIM **A602** (2009) 438









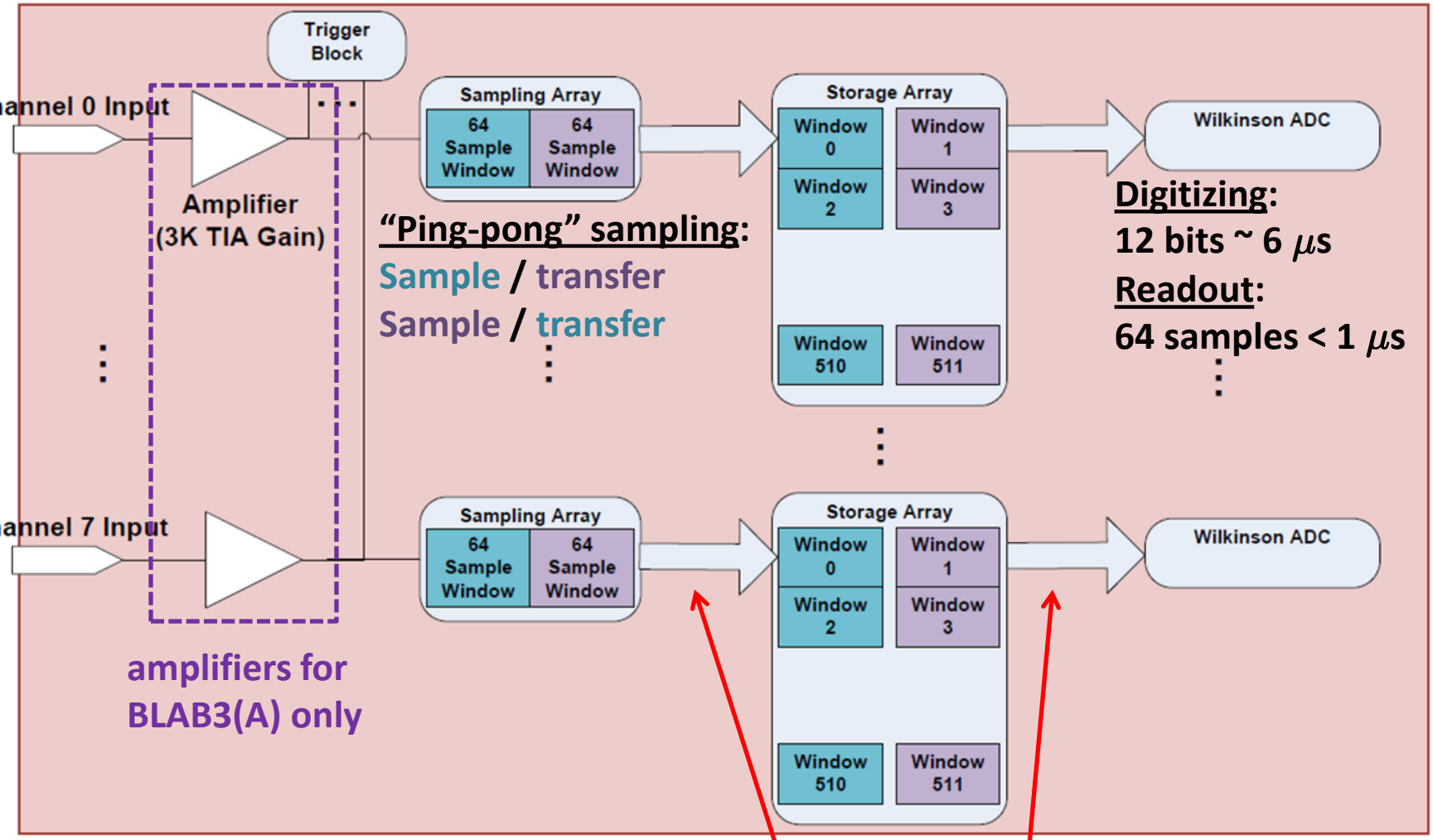
*** But only one channel / chip…**

Ice Radio Sampler (IRS2) / Buffered LABRADOR 3 (BLAB3A) Specifications

32768	samples/chan (8-32us trig latency)
8	channels/IRS ASIC
8	Trigger channels
~9	bits resolution (12-bits logging)
64	samples convert window (~16-64ns)
1-4	GSa/s
1	word (RAM) chan, sample readout
16	us to read all samples
100's	Hz sustained readout (multibuffer)

- Difference between IRS/BLAB
  - BLAB has input amplifier
  - ~~IRS doesn't really use internal trigger capability~~

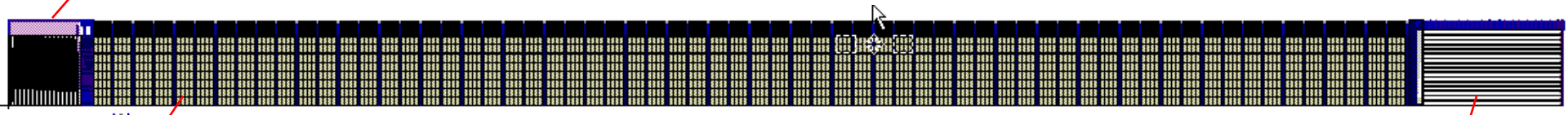
Basic Architecture

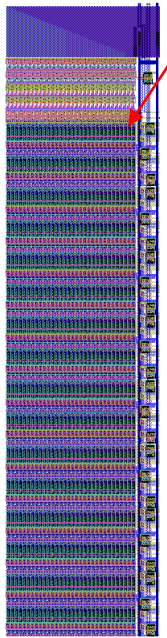


IRS/BLAB3
Single Channel

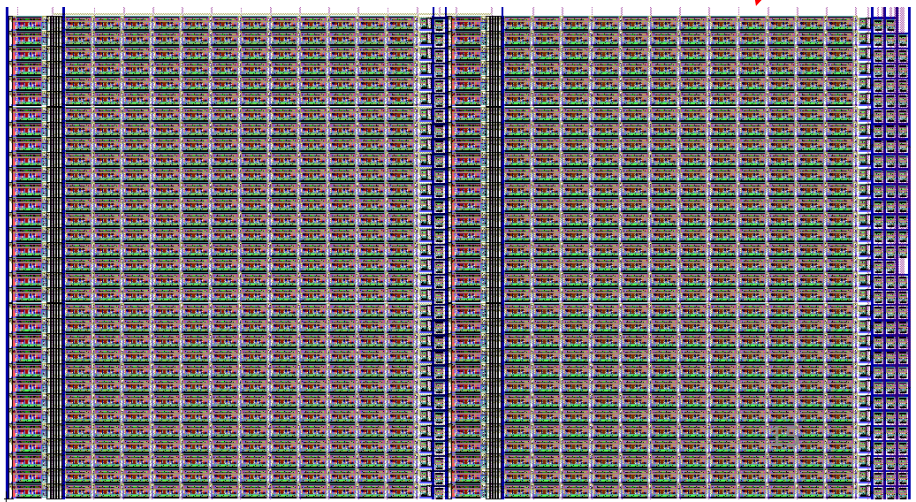
- Sampling: 128 (2x 64) separate transfer lanes

Recording in one set 64, transferring other
("ping-pong" → "2 stage sampling")



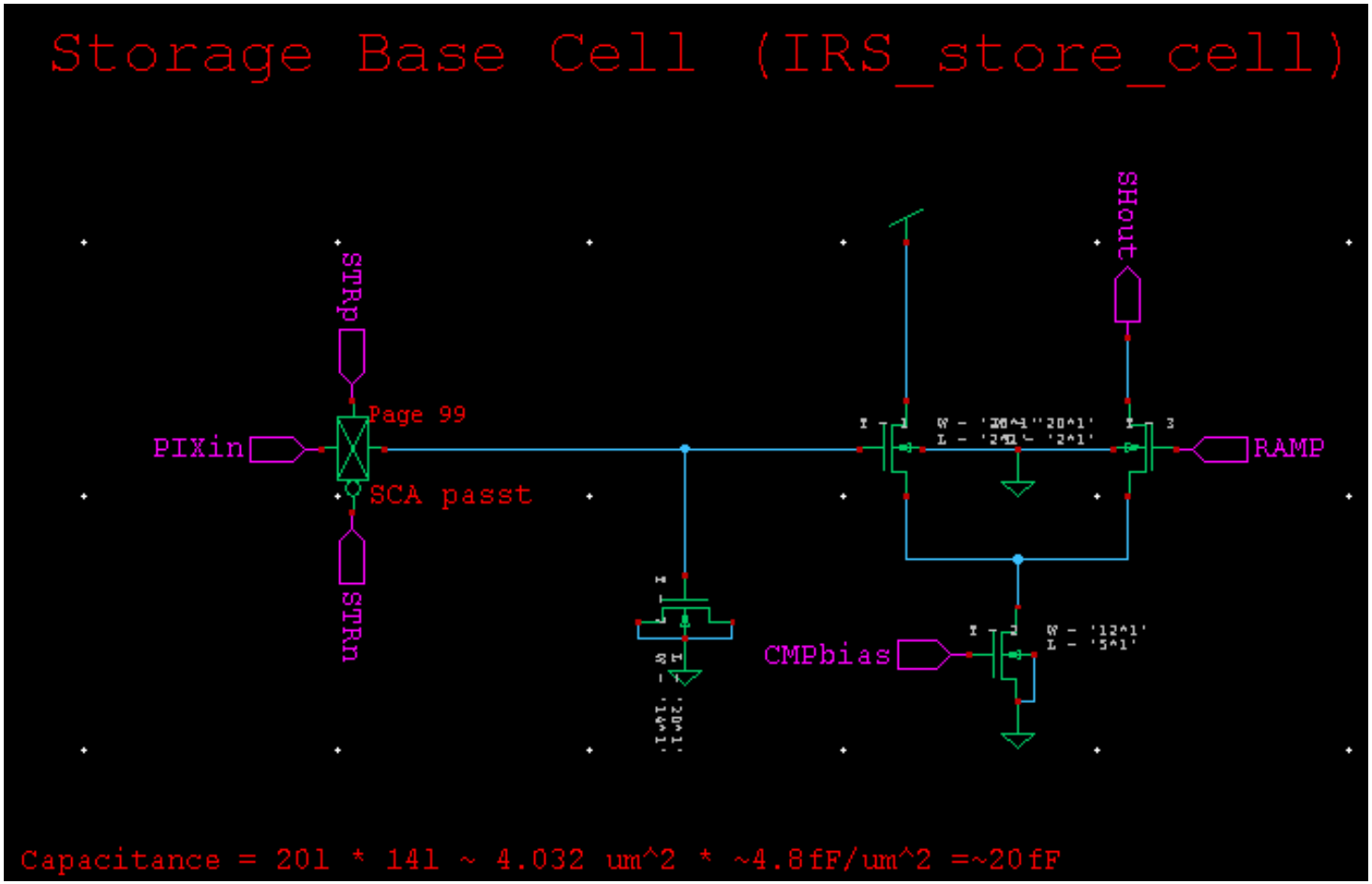


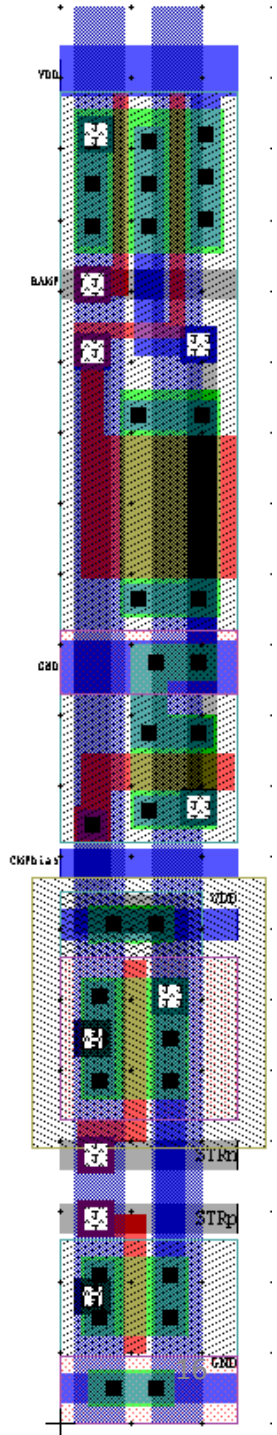
- Storage: 64 x 512 (512 = 8 * 64)



- Wilkinson (32x2): 64 conv/channel

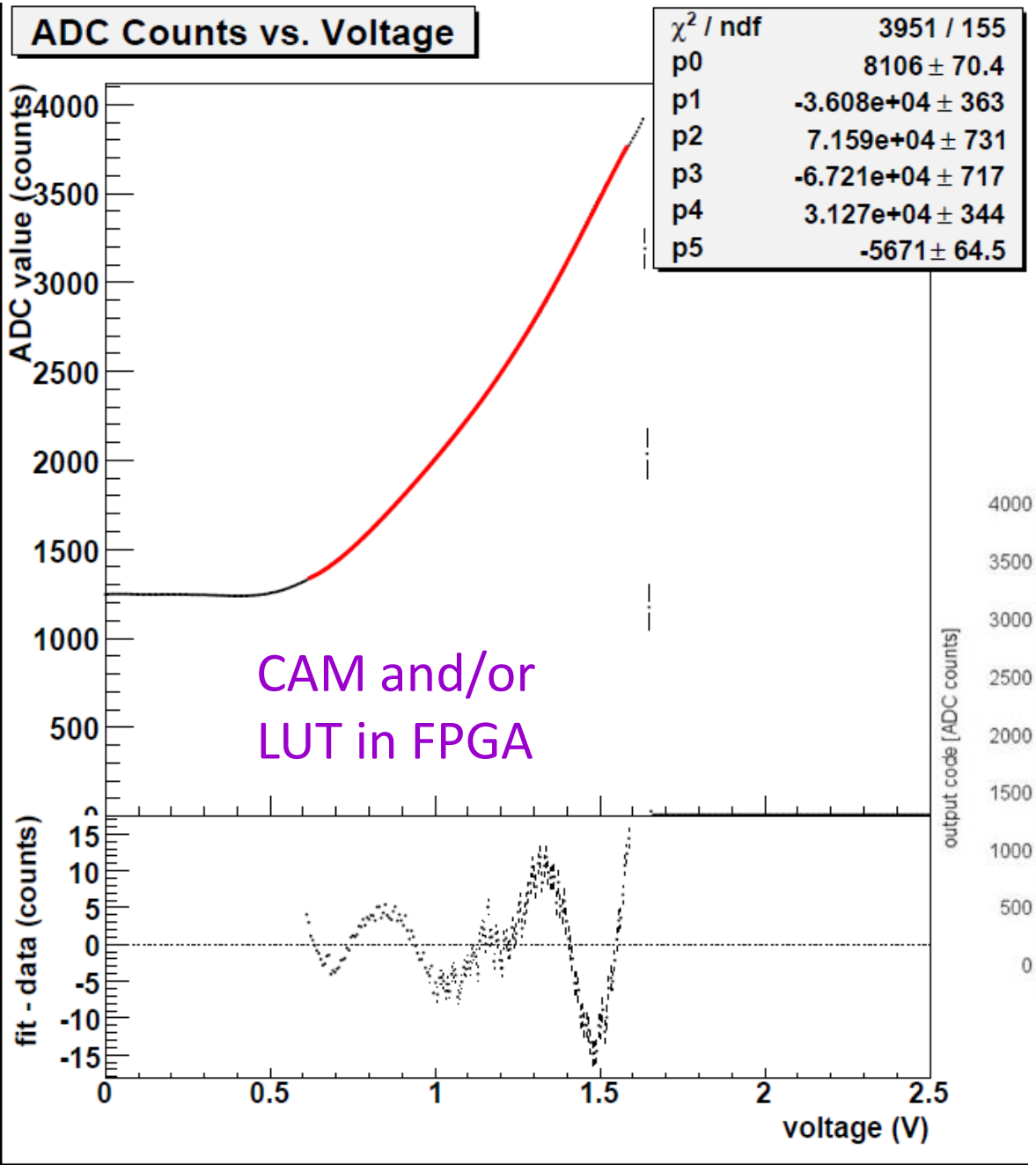
Storage Cell - compact





- Diff. Pair as comparator
  - Density ~ 25k storage cells/mm^2 (0.25um)

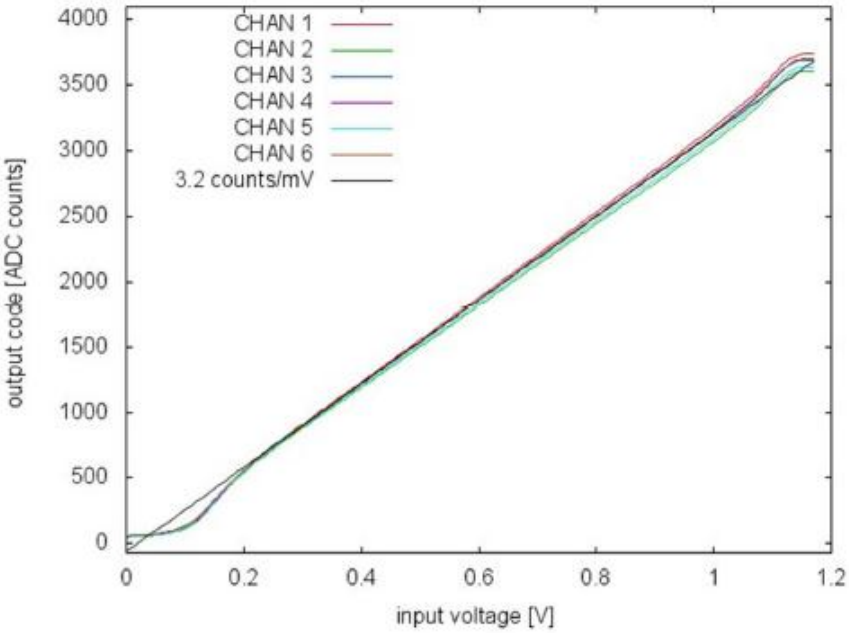
Linearity Calibration



➔ Compactness of comparator has its drawbacks…

(Left) IRS2 linearity

(Below) PSEC-4 linearity



UH Deep Buffering ASICs

- Demonstrated capability of deep analog buffering in 0.25 μm process (10 μs @ 3 GSa/s).
  - Some tradeoffs in linearity, power...
  - Detailed characterizations of these ASICs ongoing:

☑ Trigger latency is no problem.

❑ "Dead time-less" acquisition…

☑ ASIC infrastructure exists.

❑ Simultaneous sample/digitize still needs to be demonstrated.

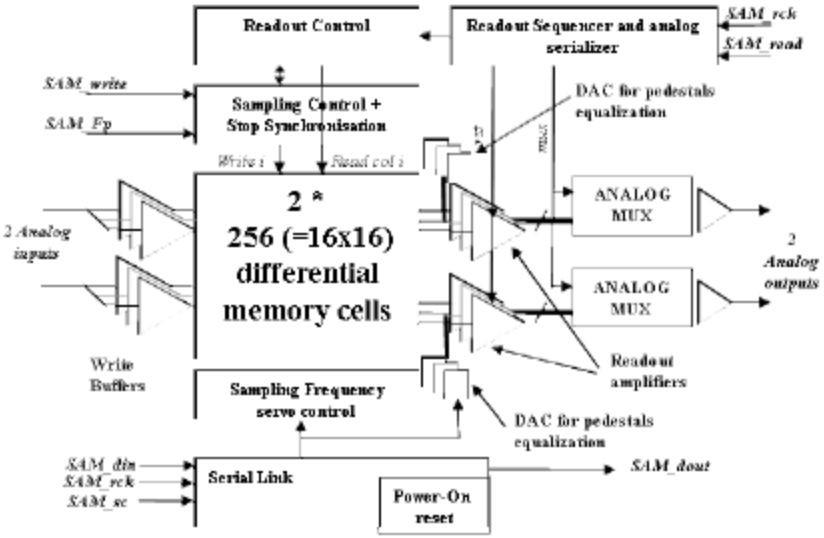
❑ High event rates will require online feature extraction.

SAM ("Swift Analog Memory")

- **SAM ("Swift Analog Memory")**

Number of ch	2 differential
Number of cells/ch	256
BW > 250 MHz	
Sampling Freq	700MHz-2.5GHz
High Readout Speed	>16 MHz
Simultaneous R/W	No
Smart Read pointer	Yes (integrate a 1/Fs step TDC)
Many modes configurable by a serial link.	
Auto-configuration @ power on	
Low cost for medium size prod=> AMS 0.35 µm	

6000 ASICs manufactured,tested and delivered in Q2 2007

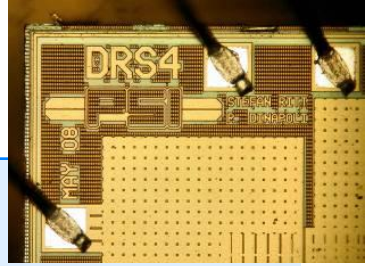


- **SAMLONG**
  - Extended buffer: 1024 samples.
  - Sampling rates up to 3.2 GSa/s.
  - Low noise (0.35 mV_{RMS})

***Both require external ADC to digitize.**

**From Eric Delagnes's talk @ January Clermont workshop.

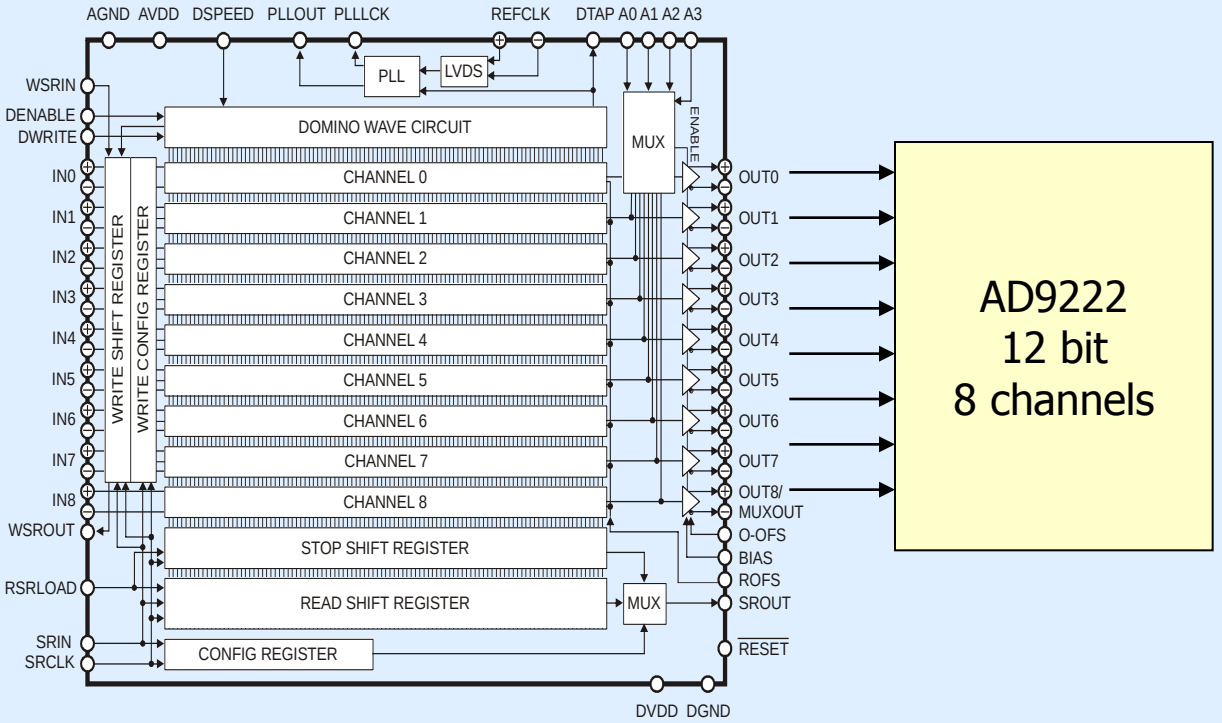
DRS4



- Fast analog readout: 30 ns / sample
- Parallel readout
- Region-of-interest readout
- Simultaneous write / read

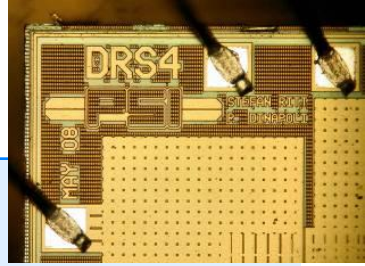
DRS4

FUNCTIONAL BLOCK DIAGRAM



AD9222
12 bit
8 channels

DRS4



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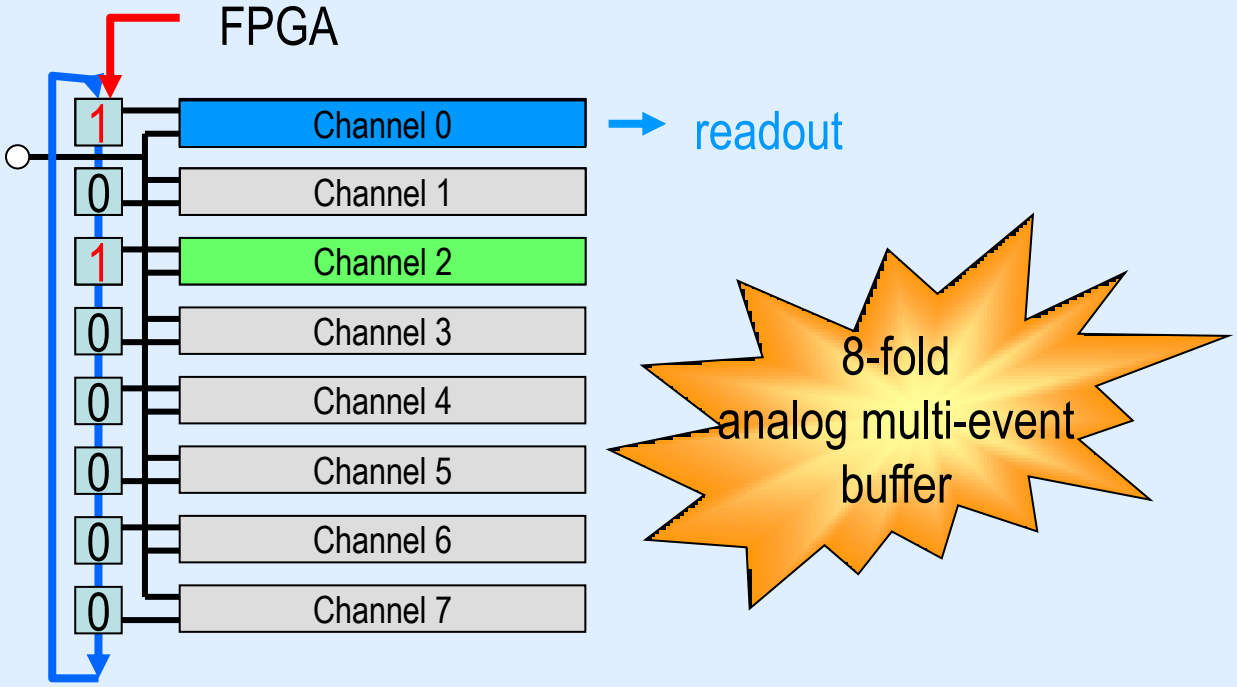
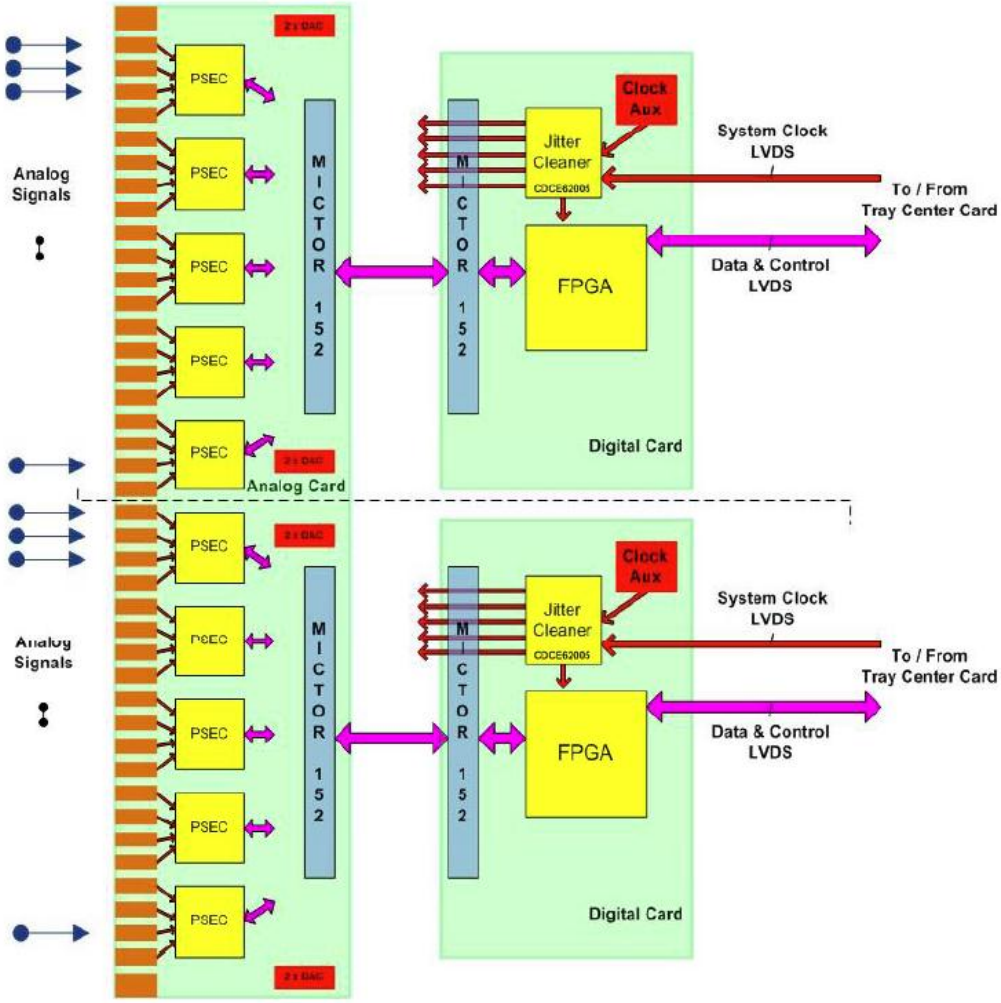


Front-end w/ Alternative ASICs

- Baseline hardware is designed around PSEC-4.
- New analog cards could be made for other ASICs as needed.
  - Are there enough/appropriate control and interface signals available?
  - Design of digital cards, central cards is ongoing now… we'll know more about the limitations soon.



Summary

- Some applications (like next generation neutrino detectors and PET) have rather different requirements:
  - Long sampling buffers.
    - ➔ Allows for long trigger latencies.
  - Continuous operation / multi-hit buffering.
    - ➔ Reduced dead time.
- Wide variety of ASICs to choose from:
  - Deep sampling being explored in ASICs from Hawaii.
  - Other ASICs (e.g., SAM, DRS4) have low noise, good response.
- In principle, LAPPD electronics is fairly flexible:
  - Can we work with a new analog card only?
  - Nice in principle, but we'll know a lot more when we try…

ASIC	Amplification?	# chan	Depth/chan	Sampling [GSa/s]	Vendor	Size [nm]	Ext ADC?
DRS4	no.	8	1024	1-5	IBM	250	yes.
SAM	no.	2	1024	1-3	AMS	350	yes.
IRS2	no.	8	32536	1-4	TSMC	250	no.
BLAB3A	yes.	8	32536	1-4	TSMC	250	no.
TARGET	no.	16	4192	1-2.5	TSMC	250	no.
TARGET2	yes.	16	16384	1-2.5	TSMC	250	no.
TARGET3	no.	16	16384	1-2.5	TSMC	250	no.
PSEC3	no.	4	256	1-16	IBM	130	no.
PSEC4	no.	6	256	1-16	IBM	130	no.

➔ **Success of PSEC3: proof-of-concept of moving toward smaller feature sizes.**

- Next DRS plans to use 110nm; next SAM plans to use 180 nm.

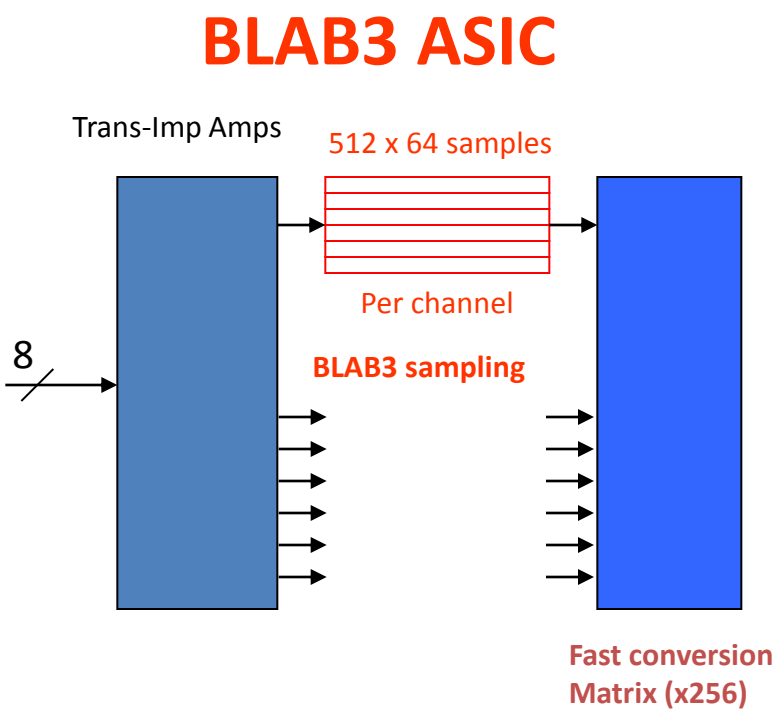
SAM/SAMLONG Specifications

NAME	SAM	SAMLONG (measured)	Unit
Power Consumption	300	160-250	mW
Sampling Freq. Range	<1to 2.5 (3.2)	0.4 to 3.2GS/s	GS/s
Analog Bandwidth	250-300 (450MHz)	400	MHz
Read Out time for a 16 cell event (2 gains 1- cells)	< 1.5	<2	µs
Fixed Pattern noise	0.4	0.35	mV rms
Total noise (constant with frequency)	0.65 (0.5mV if FPN cancelled)	0.65 (0.55mV if FPN removed)	mV rms
Maximum signal (limited by ADC range)	2 (4)	2V (ADC limited)	V
Dynamic Range	>11.6 (12.6)	>11.6	bits
Crosstalk	<3	<3	per mil
Relative non linearity	< 1	<3	%
Sampling Jitter	<15	<18	ps rms

**From Eric Delagnes's talk @ January Clermont workshop.

Hit Processing numbers

Assume:
100kHz charged track hits on each bar



~32 p.e./track (1% of 100ns windows)
30kHz trigger rate
Each PMT pair sees <8> hits
240k hits/s
Each BLAB3 has an average occupancy <1 hit (assume 1)
400ns to convert 256 samples
16ns/sample to transfer
At least 16 deep buffering
(Markov overflow probability est. < 10^{-38})

Each hit = 64samples * 8bits = 512bits
➔~125Mbits/s
(link is 3.0 Gb/s ~ x30 margin)

Improvements based upon
Lessons learned from BLAB2

Plan to model in standard queuing simulator, but looks like no problem
(CF have done same exercise with Jerry Va'vra for 150kHz L1 of SuperB and can handle rate)