PSEC-4 Waveform Digitizing ASIC + Analog Card

Front-end of SuperModule DAQ system

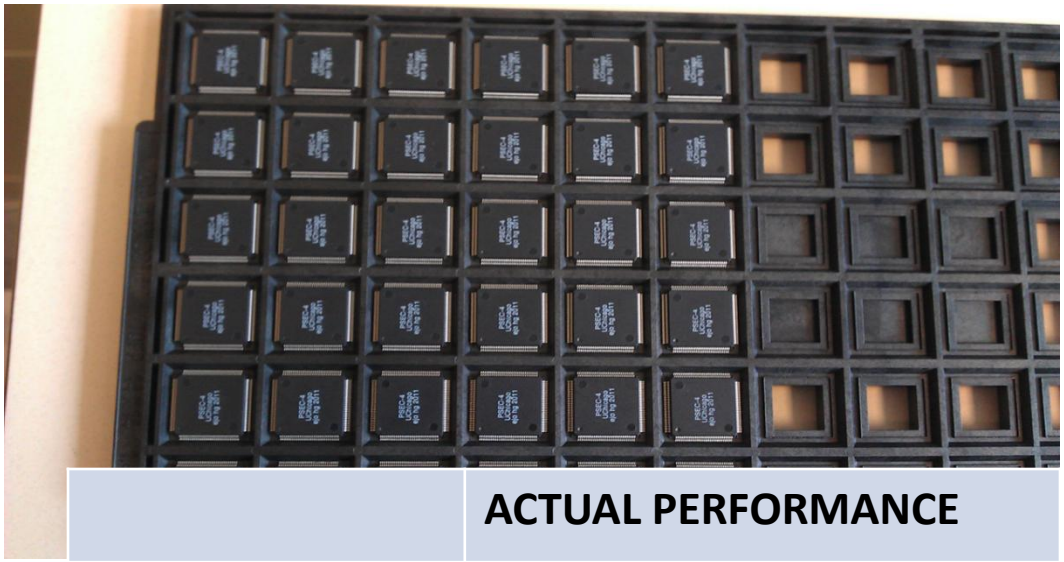
Eric Oberla

LAPPD collab meeting III

9-Dec-2011

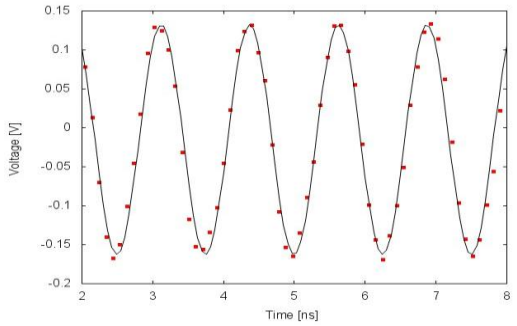
PSEC-4

- Waveform digitizing ASIC
- Sampling rate capability > 10GSa/s
- Analog bandwidth > 1 GHz
- Medium event-rate capability (up to ~100 KHz)

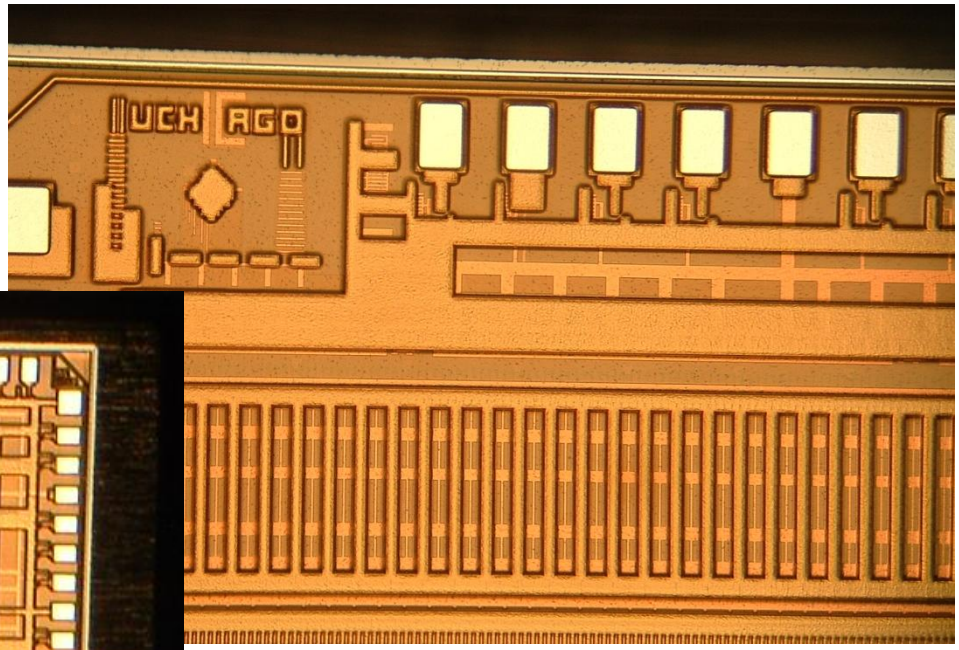


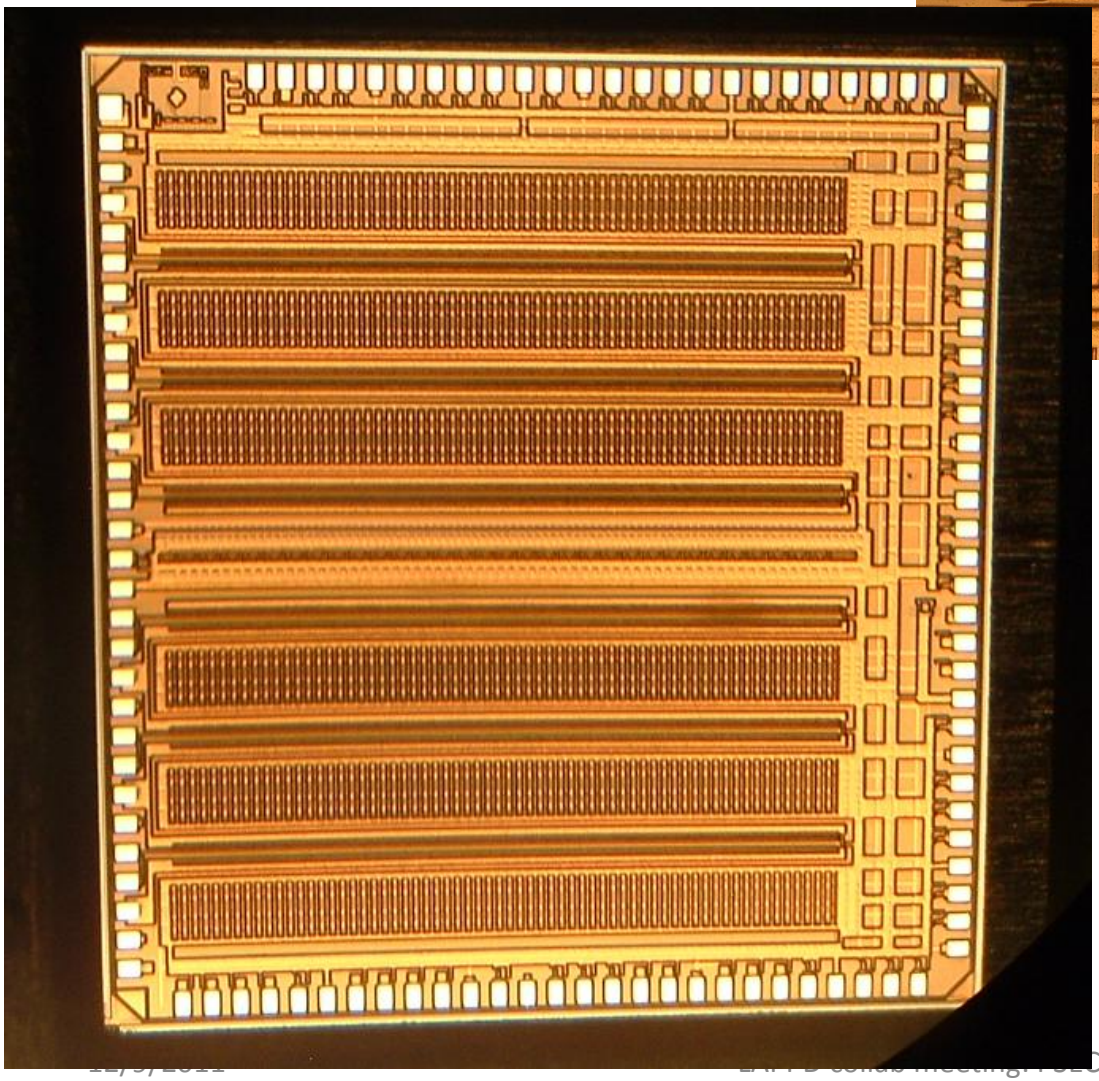
	ACTUAL PERFORMANCE
Sampling Rate	2.5-15 GSa/s
# Channels	6
Sampling Depth	256 points (17-100 ns)
Input Noise	<1 mV RMS
Analog Bandwidth	1.6 GHz
ADC conversion	Up to 12 bit @ 1.5 GHz
Dynamic Range	0.1-1.1 V
Latency	2 µs (min) – 16 µs (max)
Internal Trigger	yes

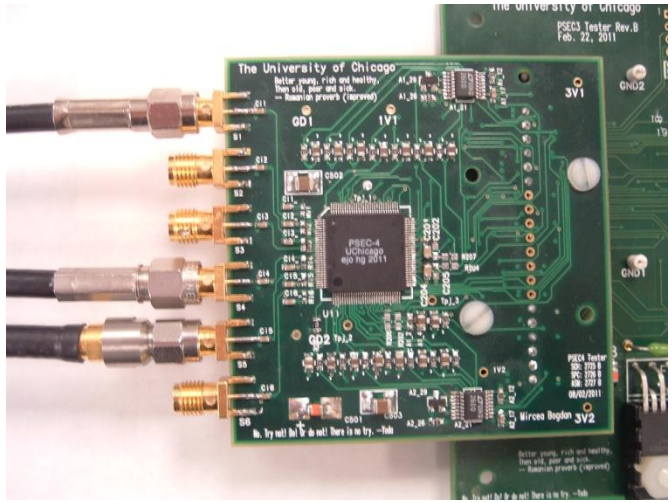
800MHz sine @ 13.3 GS/s



PSEC-4

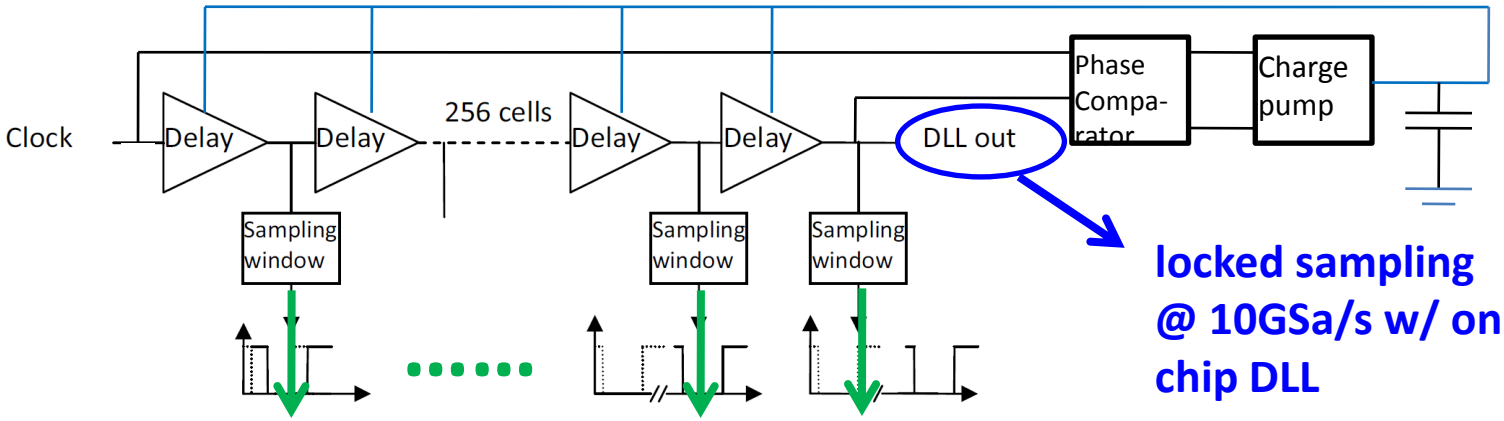

UCH AGO




The University of Chicago
PSEC4 Tester Rev.B
Feb. 22, 2011
PSEC-4
UChicago
ejo hg 2011
Mircea Bogdan 3V2

PSEC-4 architecture

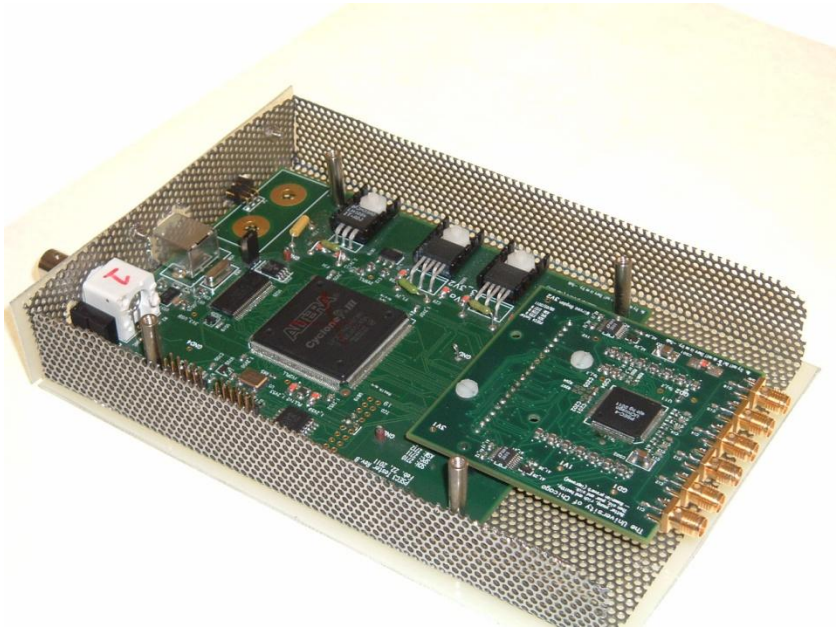
Timing generation with a delay locked loop (DLL):

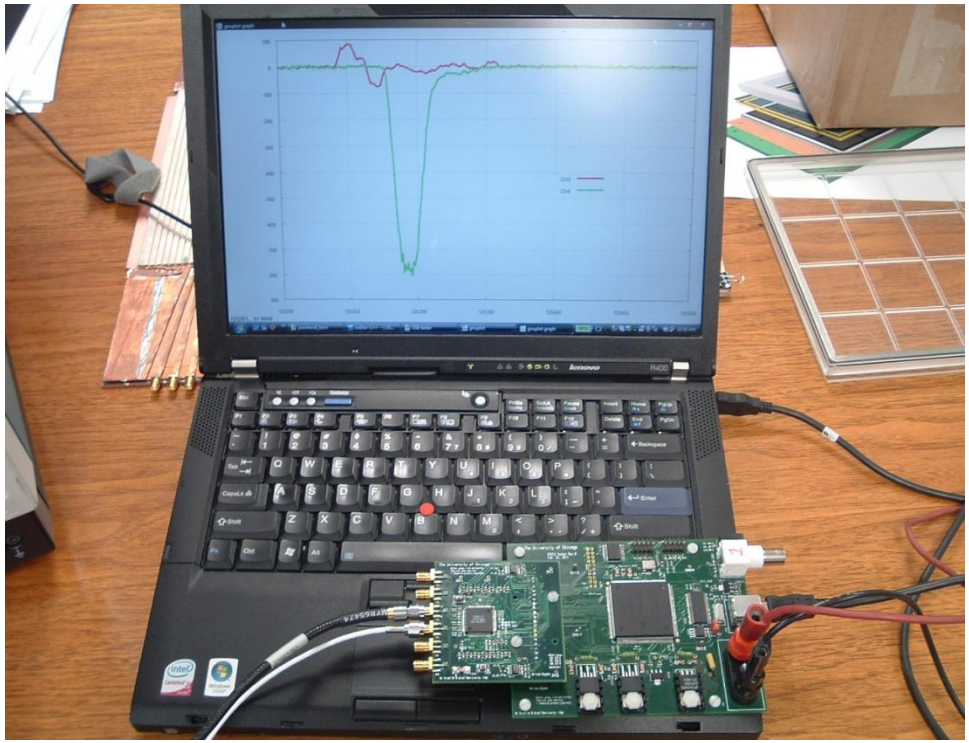


- 1536x parallel Wilkinson ADC (entire chip)
- Region of interest readout (40 MHz) -> data to FPGA

Evaluation Card

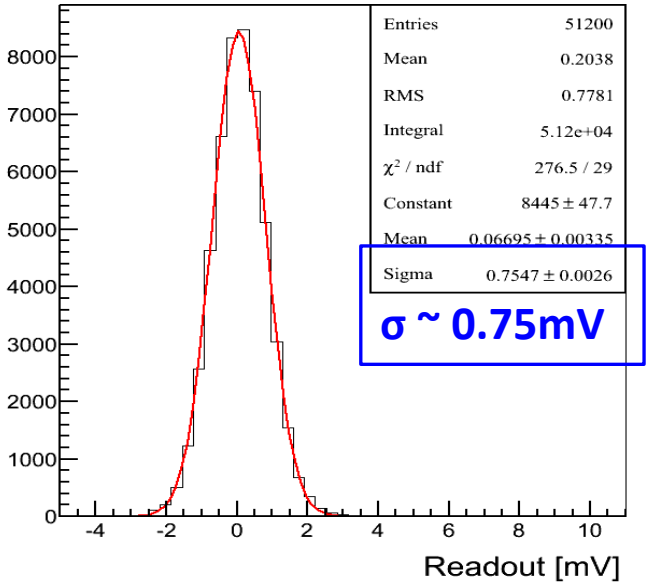
- 4 boards made (3 available in this time zone)
  - 6 channels (1 PSEC-4) per board
- USB 2.0 interface
  - Current firmware revision – 2
  - Acquisition software available with oscilloscope GUI





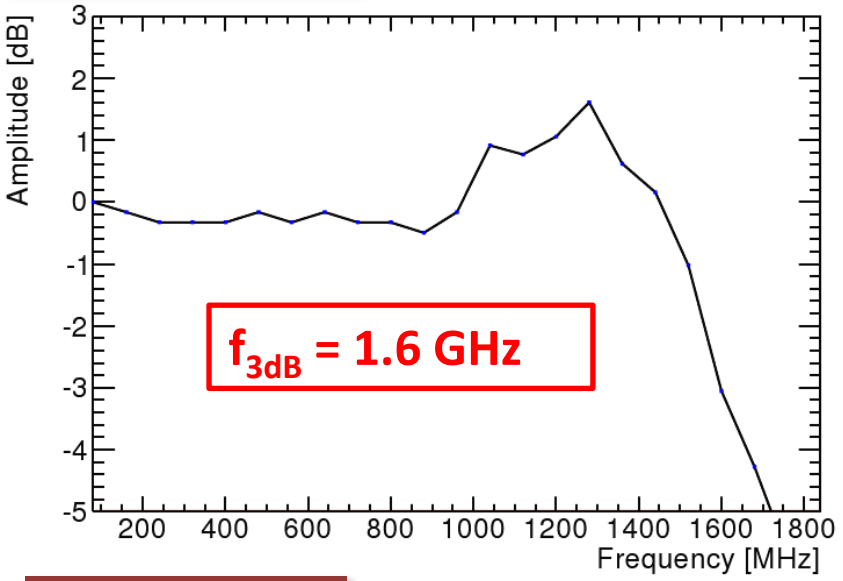
PSEC-4 Performance

Noise

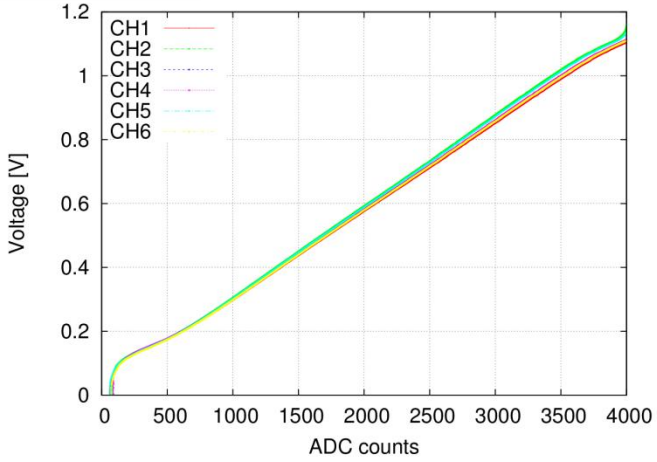


- **Low noise <1 mV**
- **~1V dynamic range with excellent linearity**
- **Analog bandwidth of 1.6 GHz**
- **Sampling rates up to 15 GSa/s**

Frequency Response

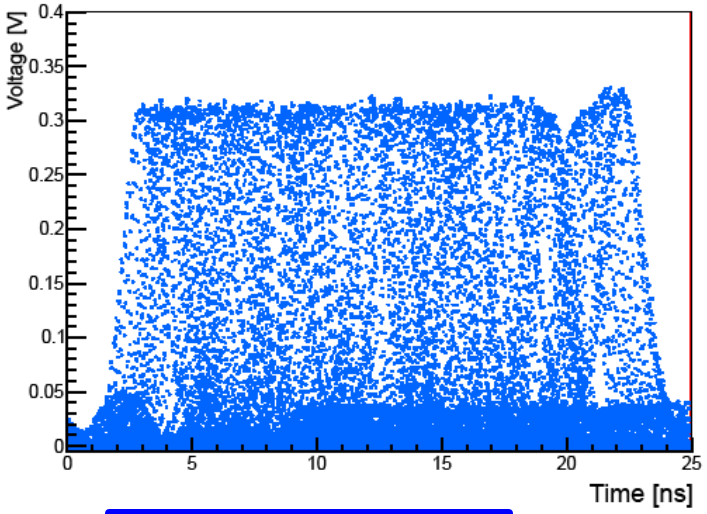


DC Response



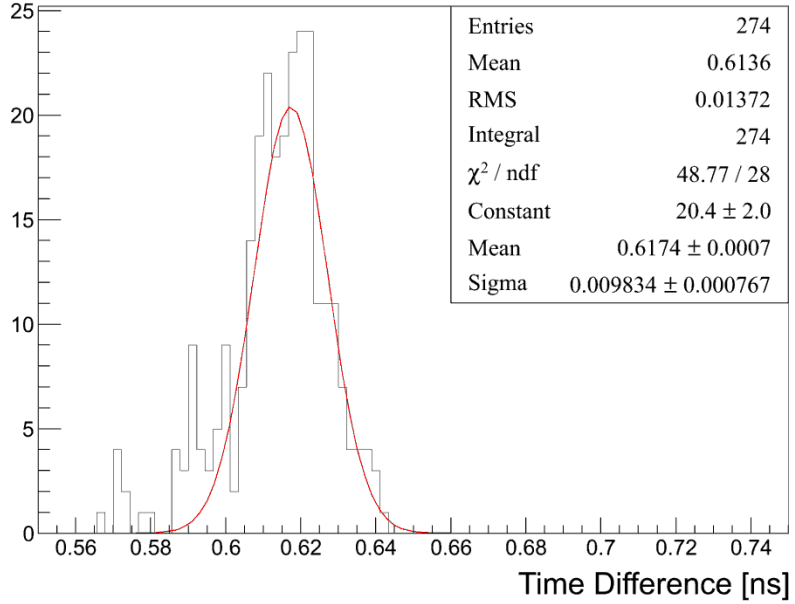
PSEC-4 timing (preliminary)

- Without time base calibration (assuming nominal 100 ps per sample interval)
- Time jitter measured at DLL output ~ 13 ps
- Sample several hundred Gaussian waveforms on 2 channels :



Data from 1 channel shown

2 -channel timing (over entire window ~10ps sigma)



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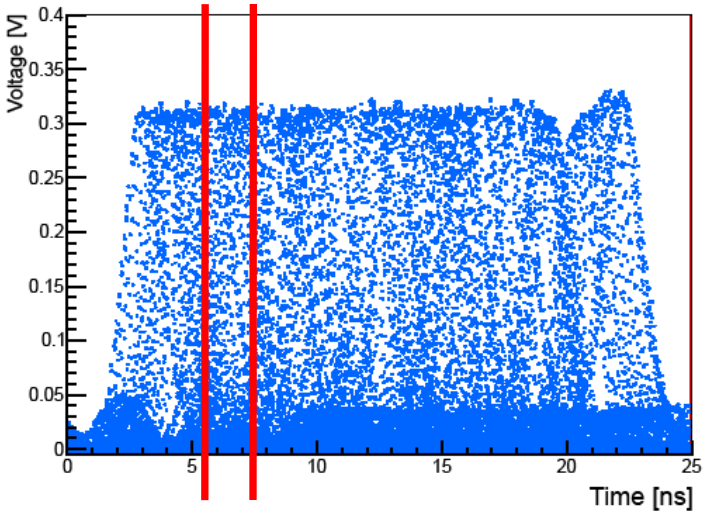
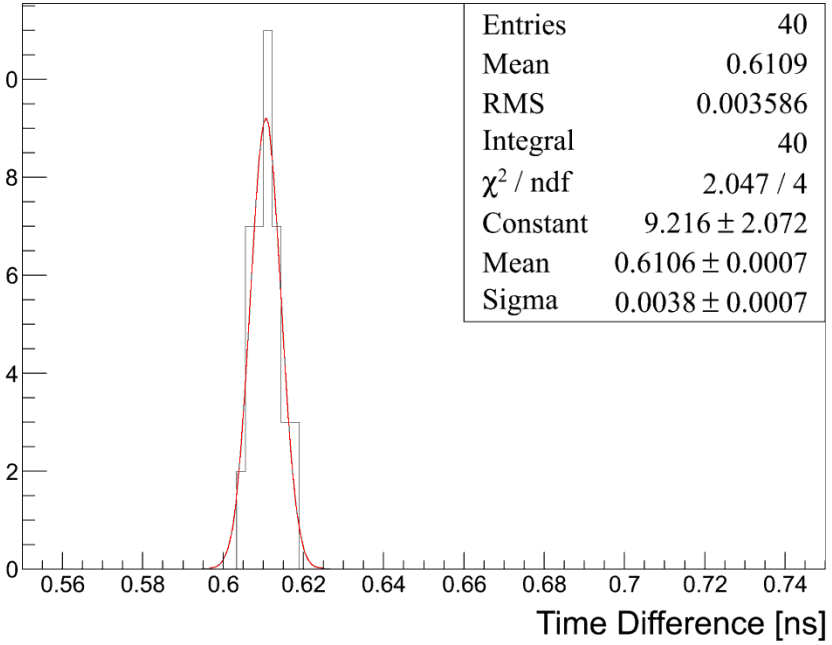


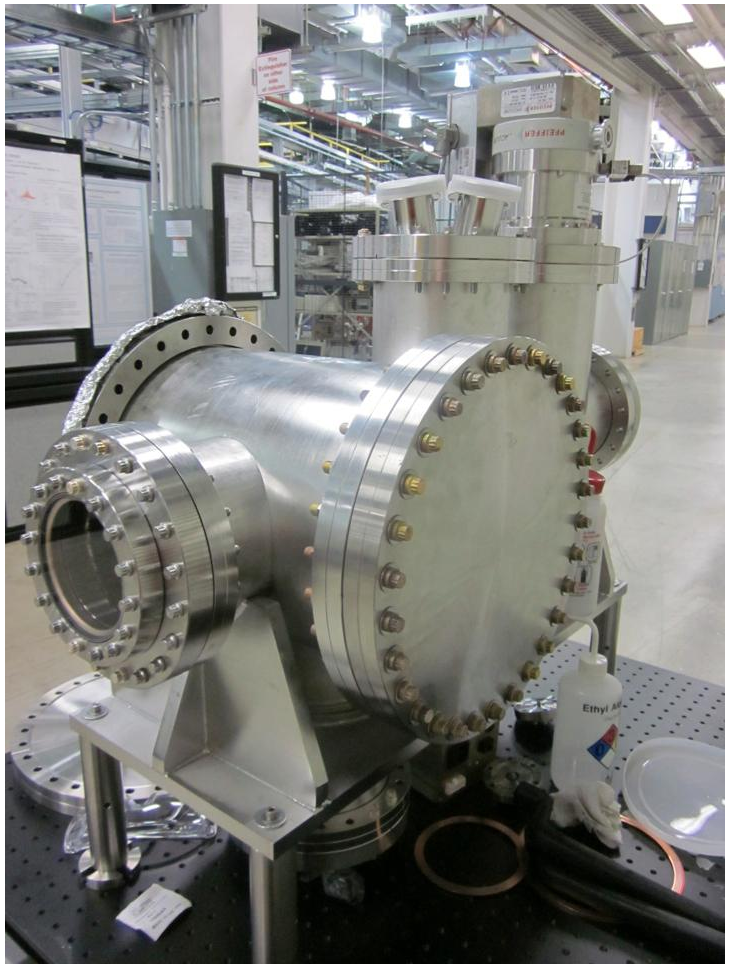
2 channel timing (window subset - 3.8ps sigma)

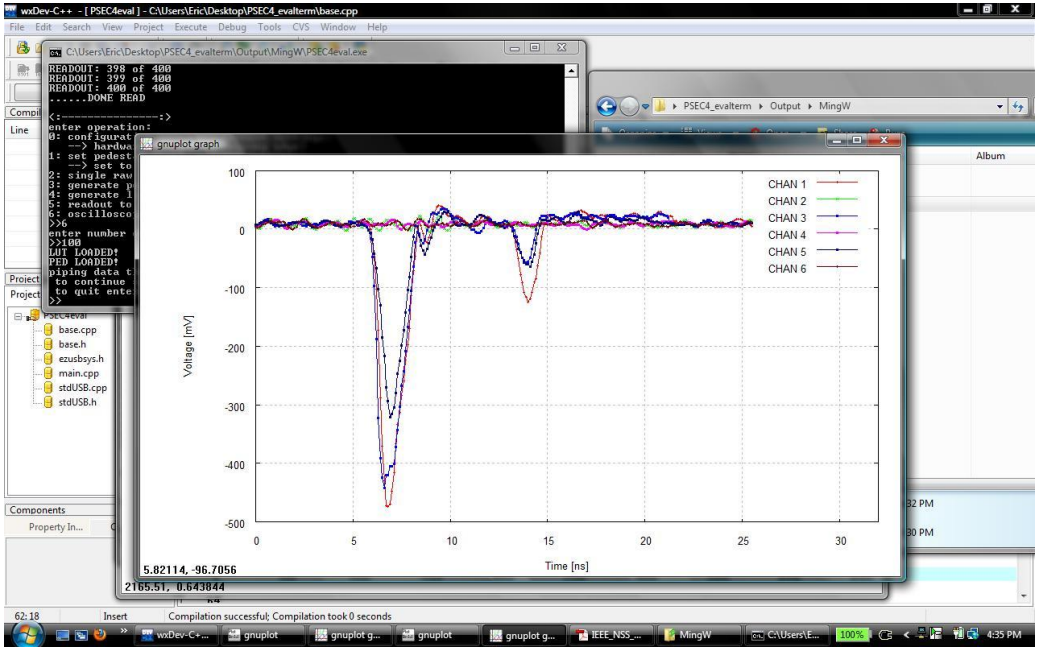


Working out various time-base calibration methods with Kurtis Nishimura (UH) -- should be implemented soon!

Argonne Test Stand

- Working to implement PSEC-4 eval at laser lab (APS)

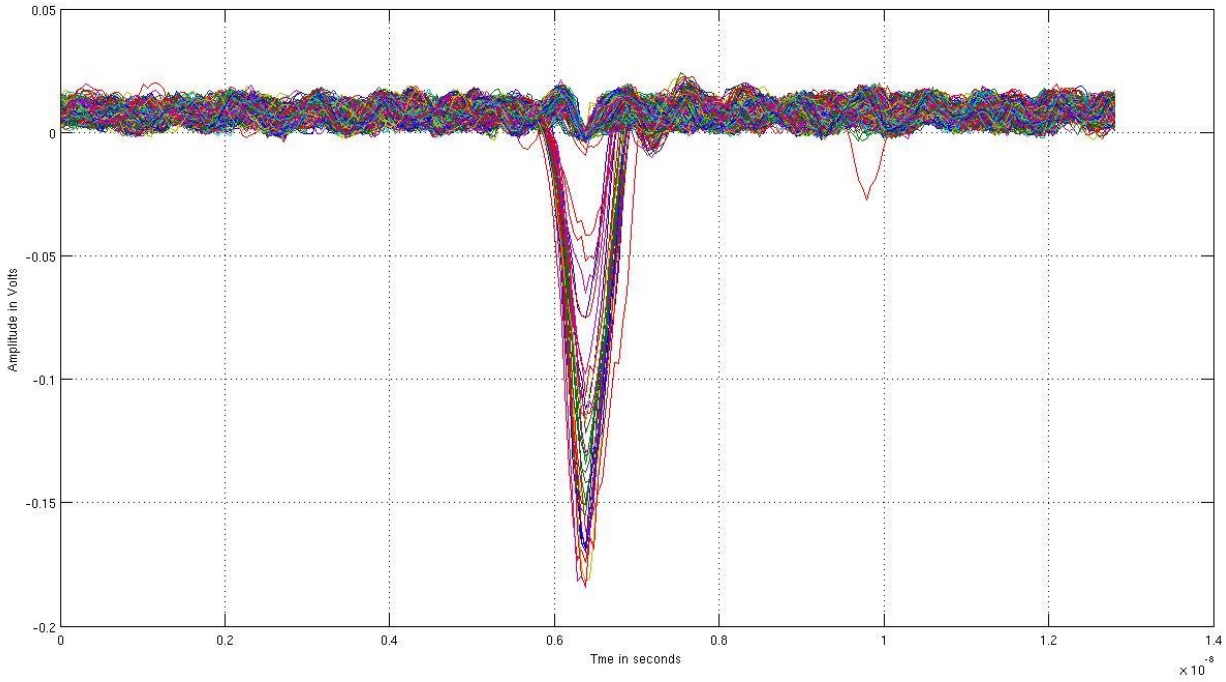




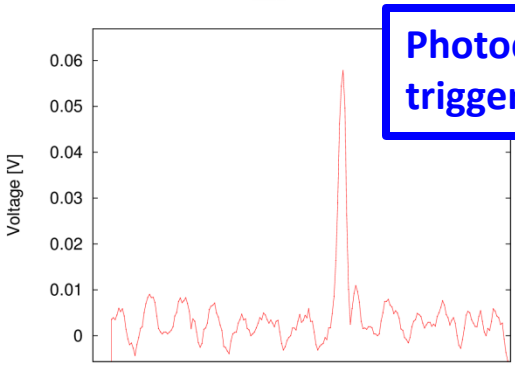
First pulses from 33mm MCP set-up captured with PSEC-4 @ 10GS/s

Argonne Test Stand

- Some 33 mm MCP pulses :



- Still some noise/triggering issues to resolve before using PSEC-4 data for analysis. Coming soon…

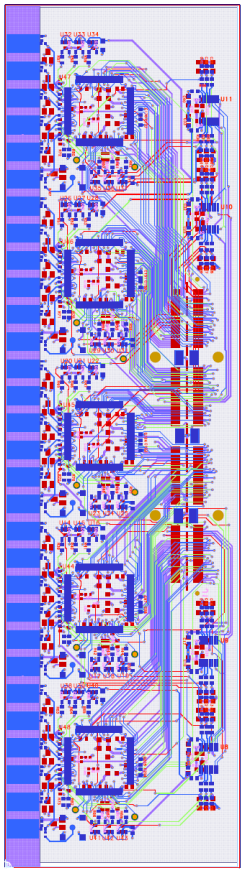


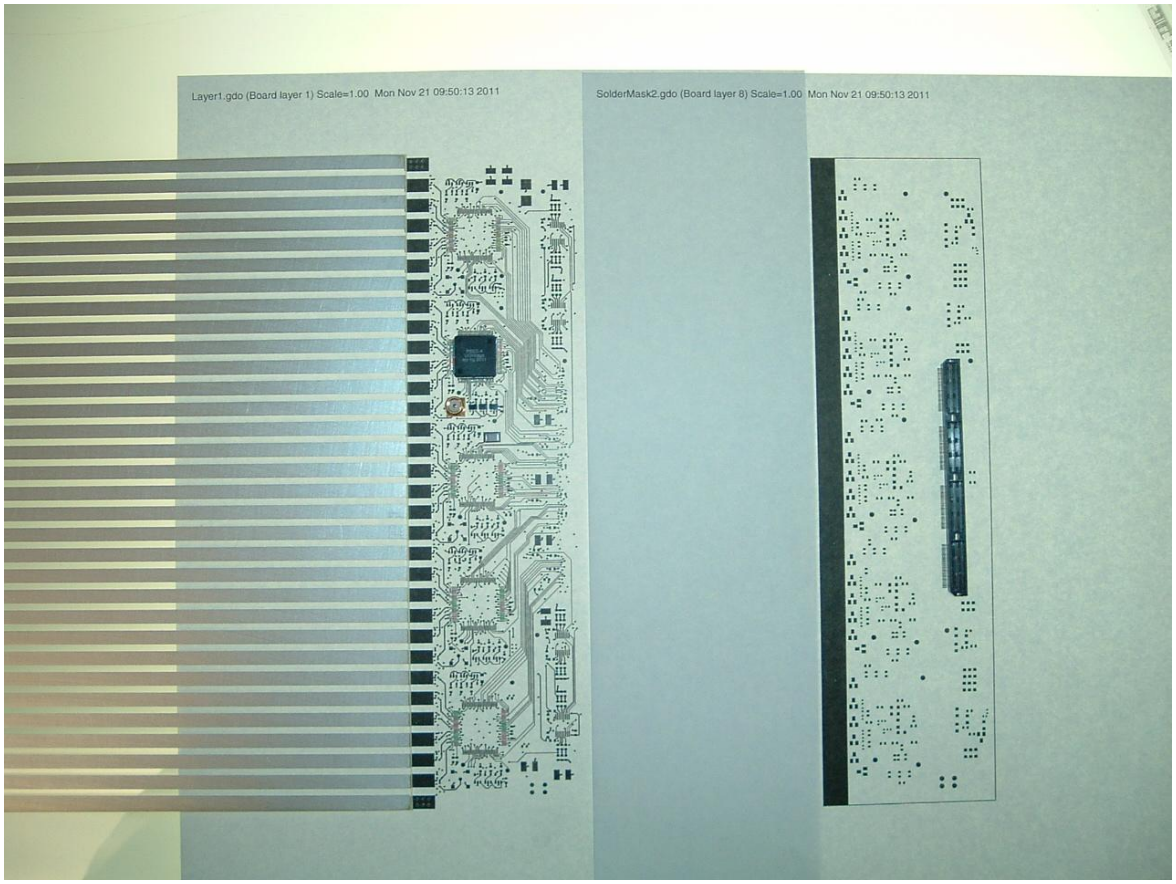
Photodiode trigger

Analog Card

- 30 chan. PSEC-4 readout board, input matched to 30 strip anode
- Digital I/O and Power thru 240 pin SAMTEC (→ digital card)

--boards due back next week--





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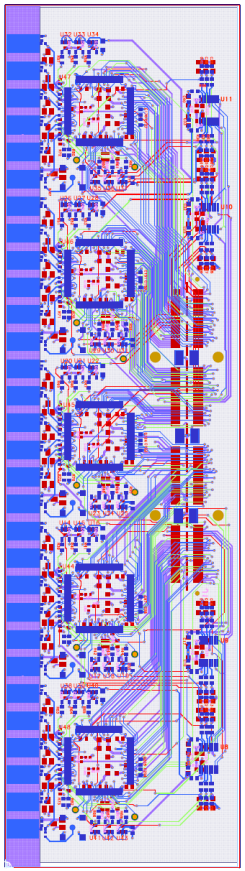
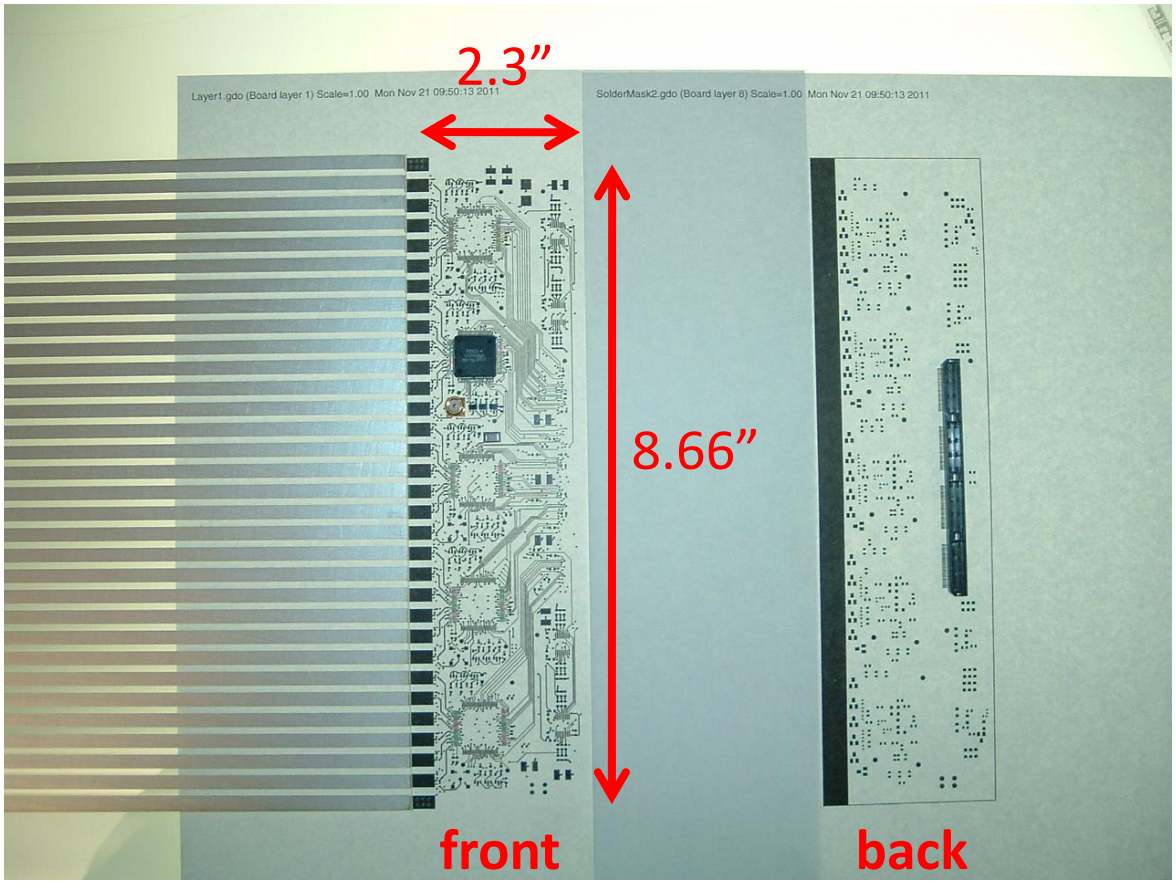
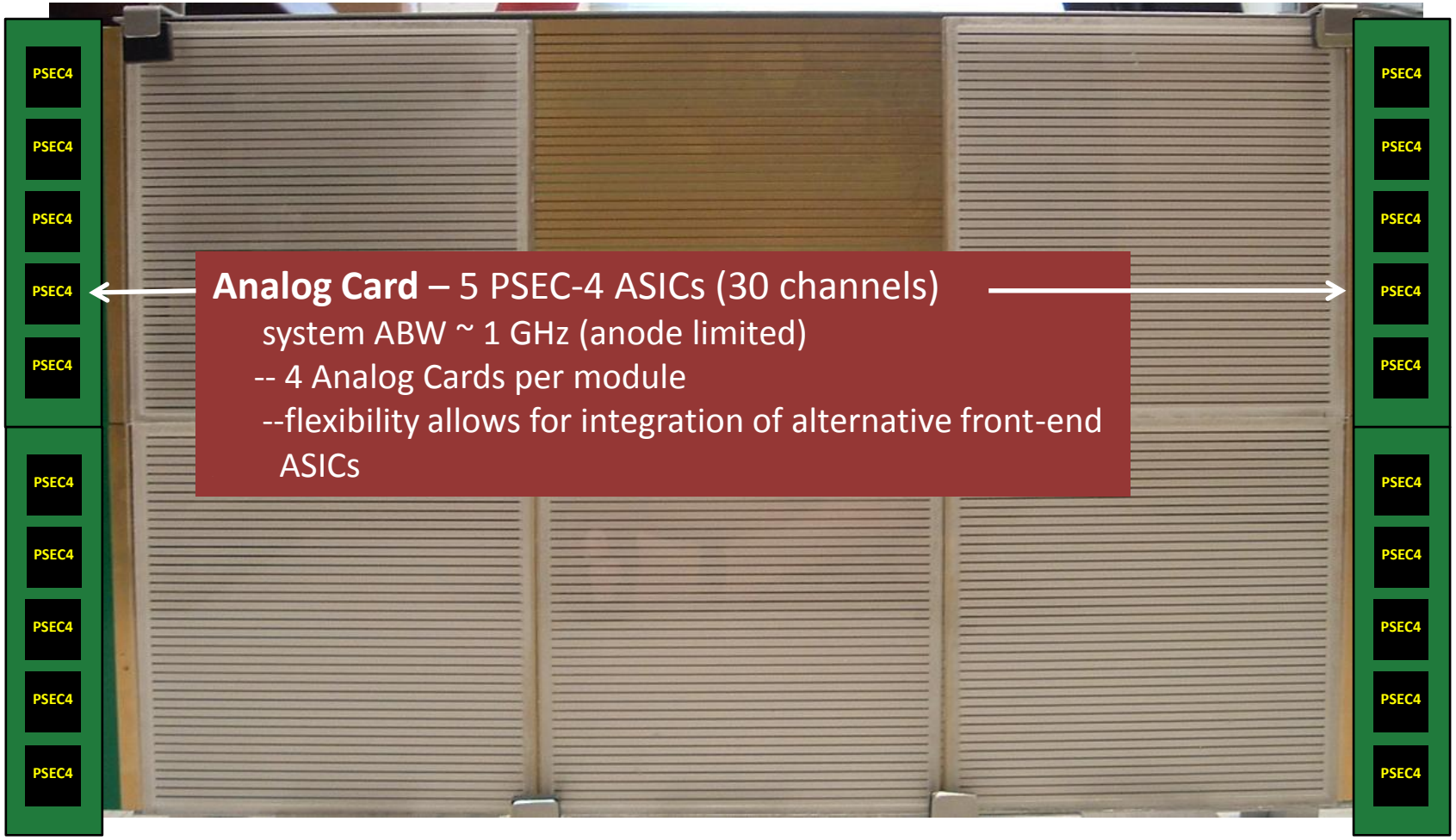




Analog Card →Super Module



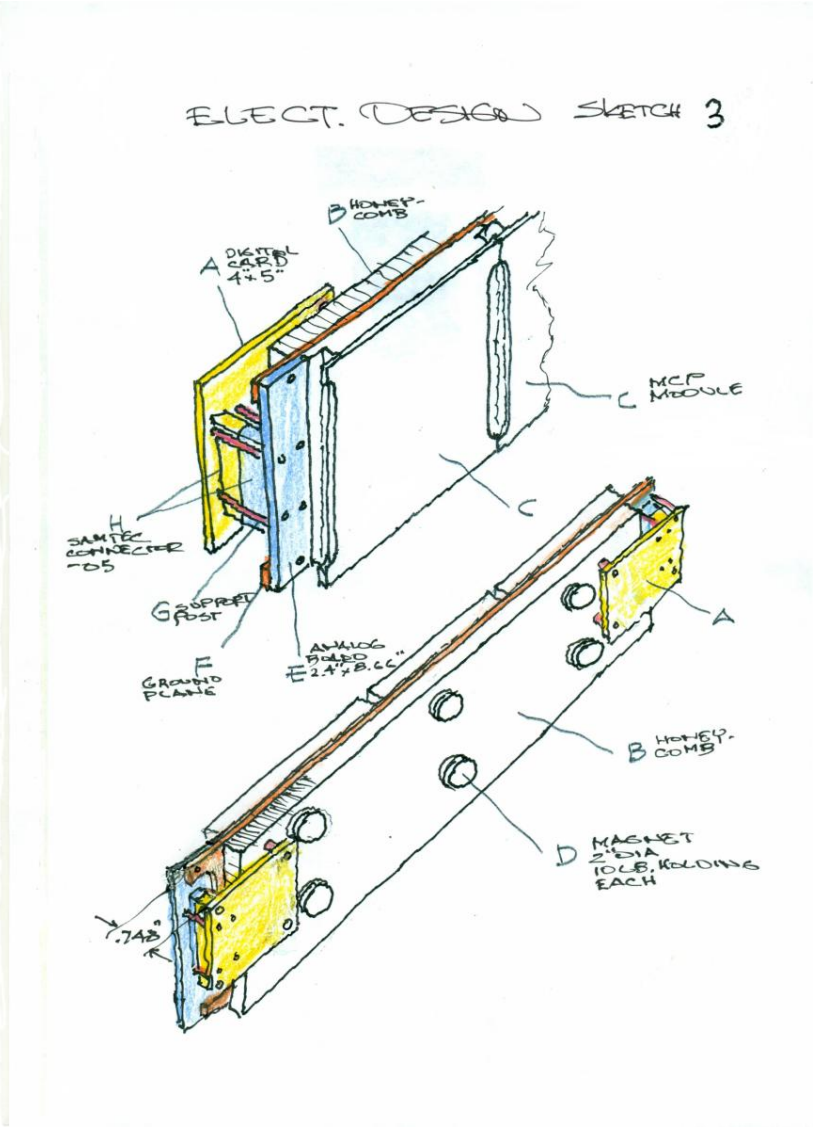
Analog Card – 5 PSEC-4 ASICs (30 channels)

system ABW ~ 1 GHz (anode limited)

-- 4 Analog Cards per module

--flexibility allows for integration of alternative front-end ASICs

Analog Card → Super Module



Analog (blue)+ Digital (yellow) cards mechanical mounting

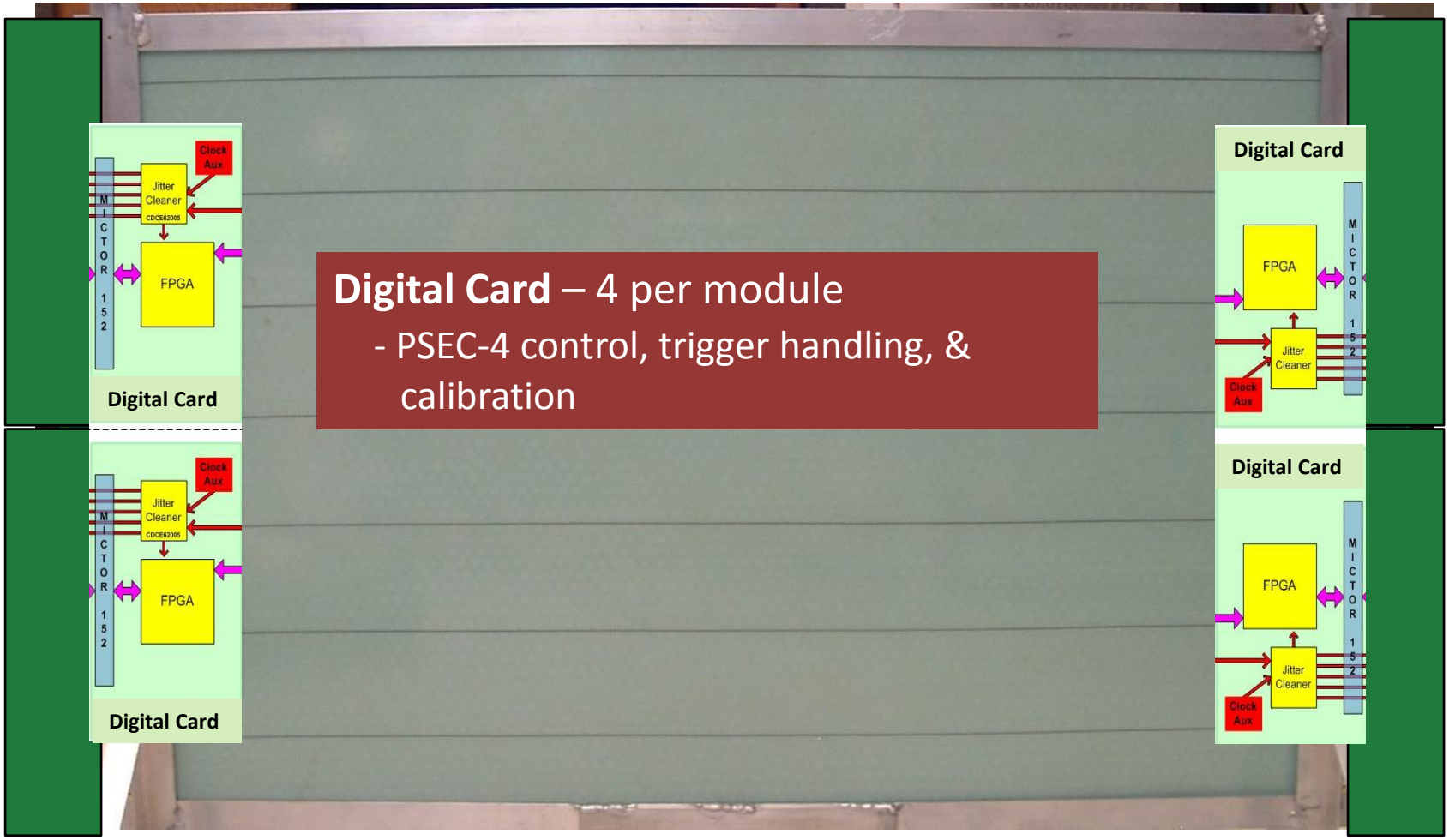
Drawing courtesy of Rich Northrup

Summary/plans

- PSEC-4 performance meets initial project goals of a (functional) high bandwidth, fast sampling ASIC
- Continued performance testing →paper
- More data runs w/ 33mm & 8 inch MCP setup
  - Integration of PSEC-4 data into analysis pipeline
  - Any necessary firmware improvements
  - Start PSEC-4/scope analysis comparison
- **Analog Card** back next week – waiting on digital card for full system testing, but preliminary tests/integration by the end of the year
- PSEC-5? Adding a deeper buffer and faster readout speed desired (reduce chip deadtime)

DAQ system

- Backside of Super Module:



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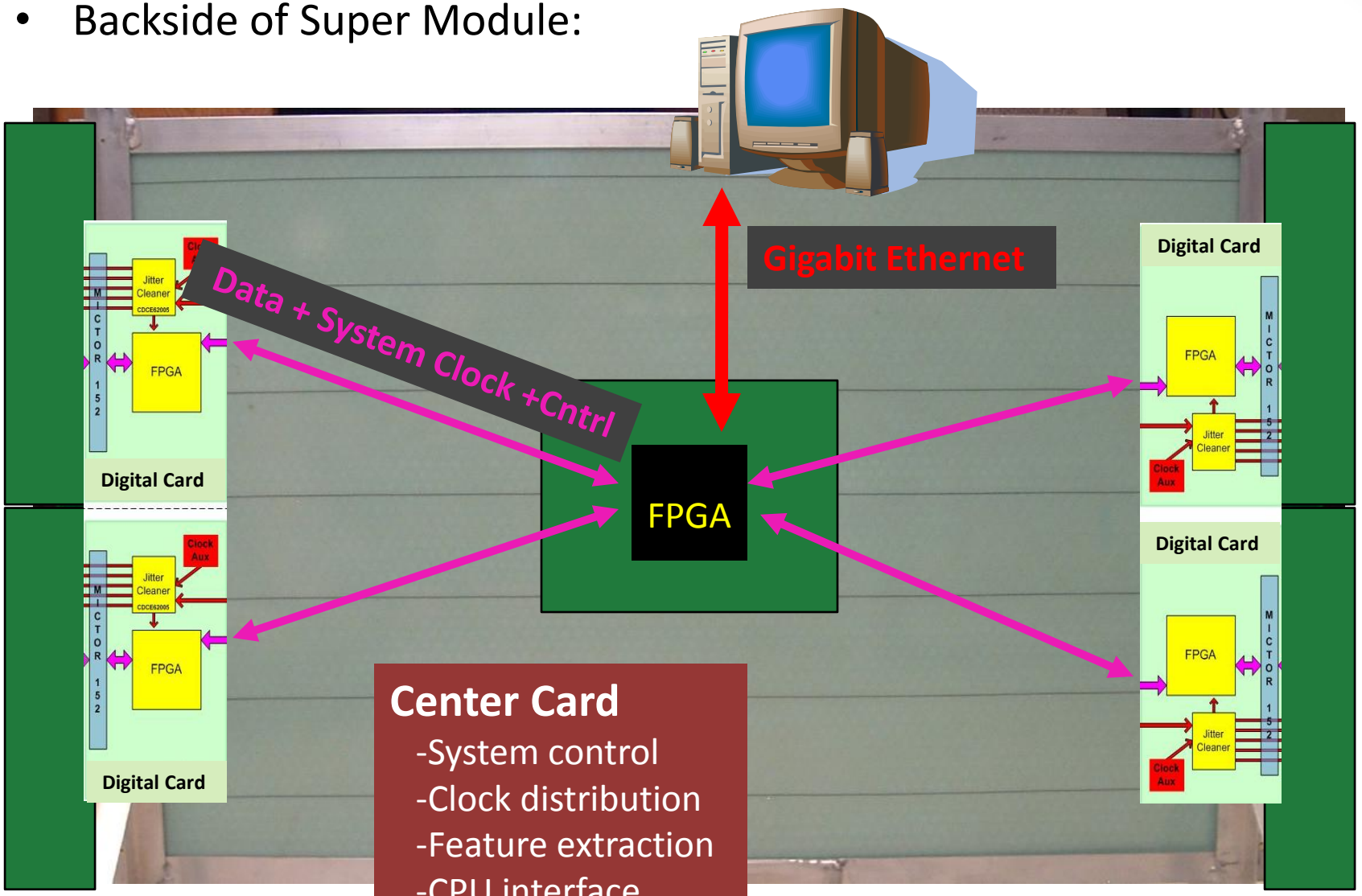
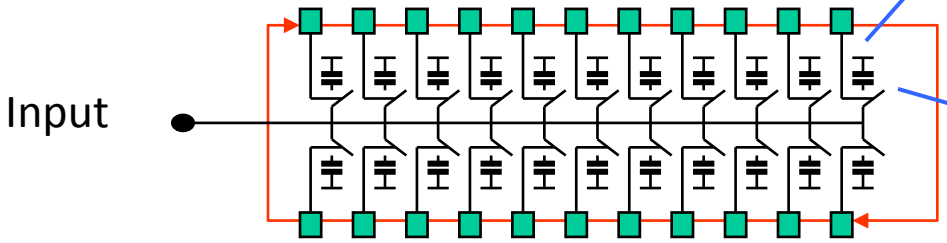
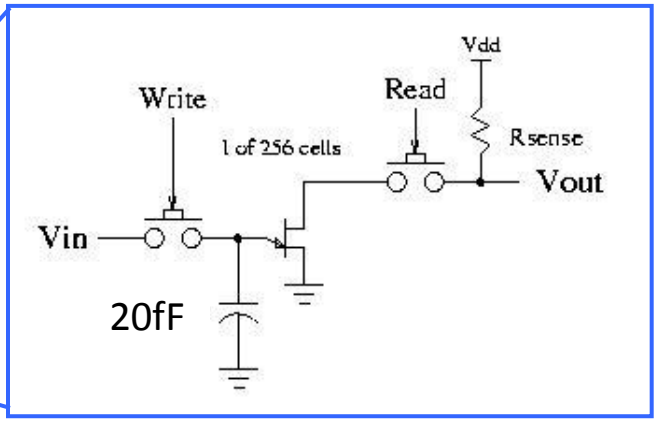


Switched Capacitor Array Sampling

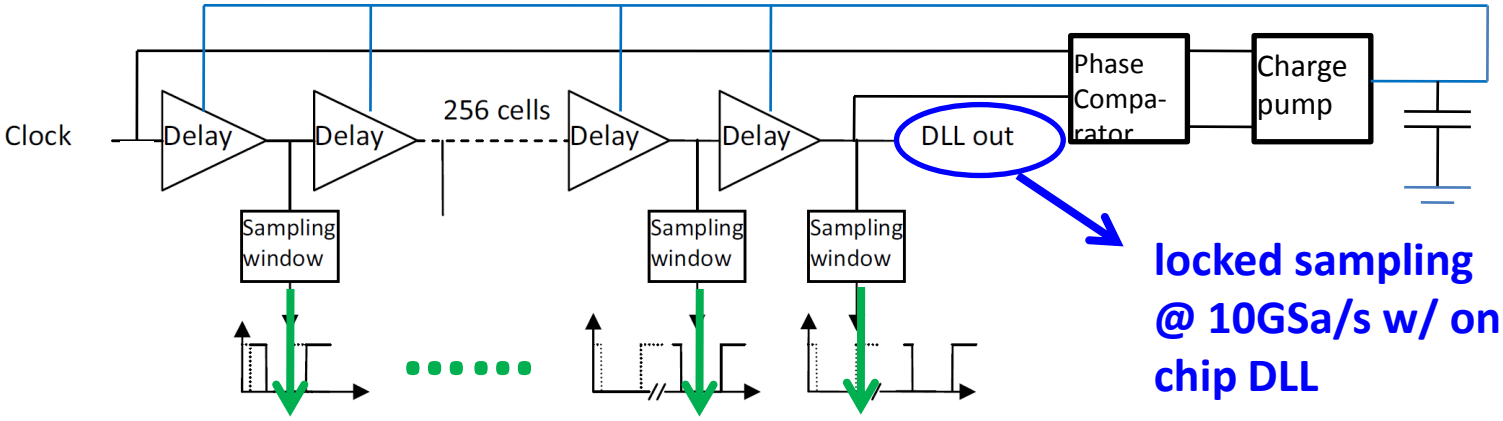
Write pointer passed along array - generates 'sampling window' (~5-10 switches closed at once):





Tiny charge: 1mV ~ 100e$^-$

Timing generation with a delay locked loop (DLL):



locked sampling @ 10GSa/s w/ on chip DLL

To switched capacitor array – sample & hold

Wilkinson ADC – easy to integrate on-chip