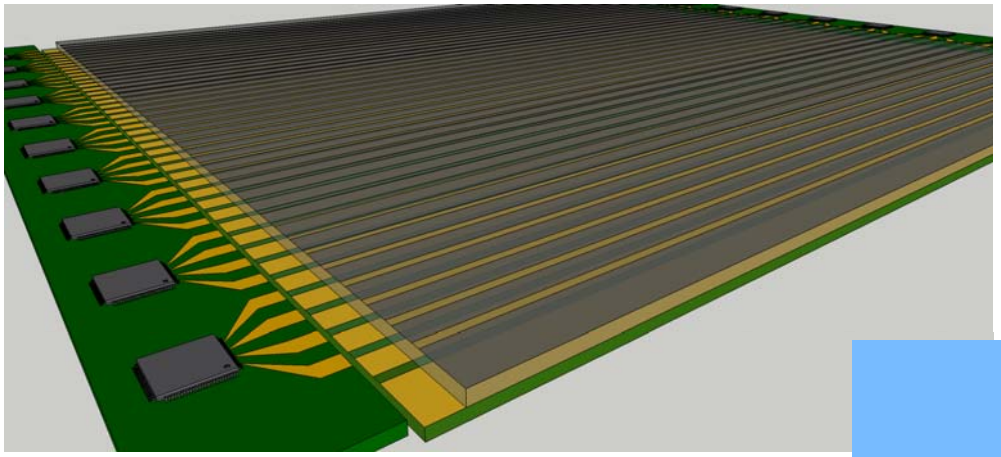
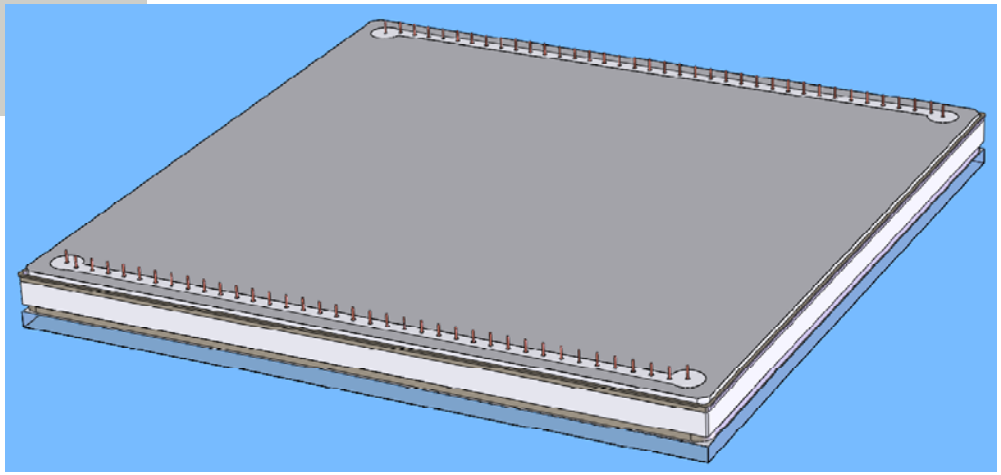
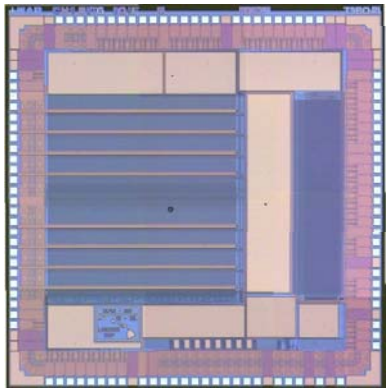
Integration of Front-End Electronics with the Ceramic Detector





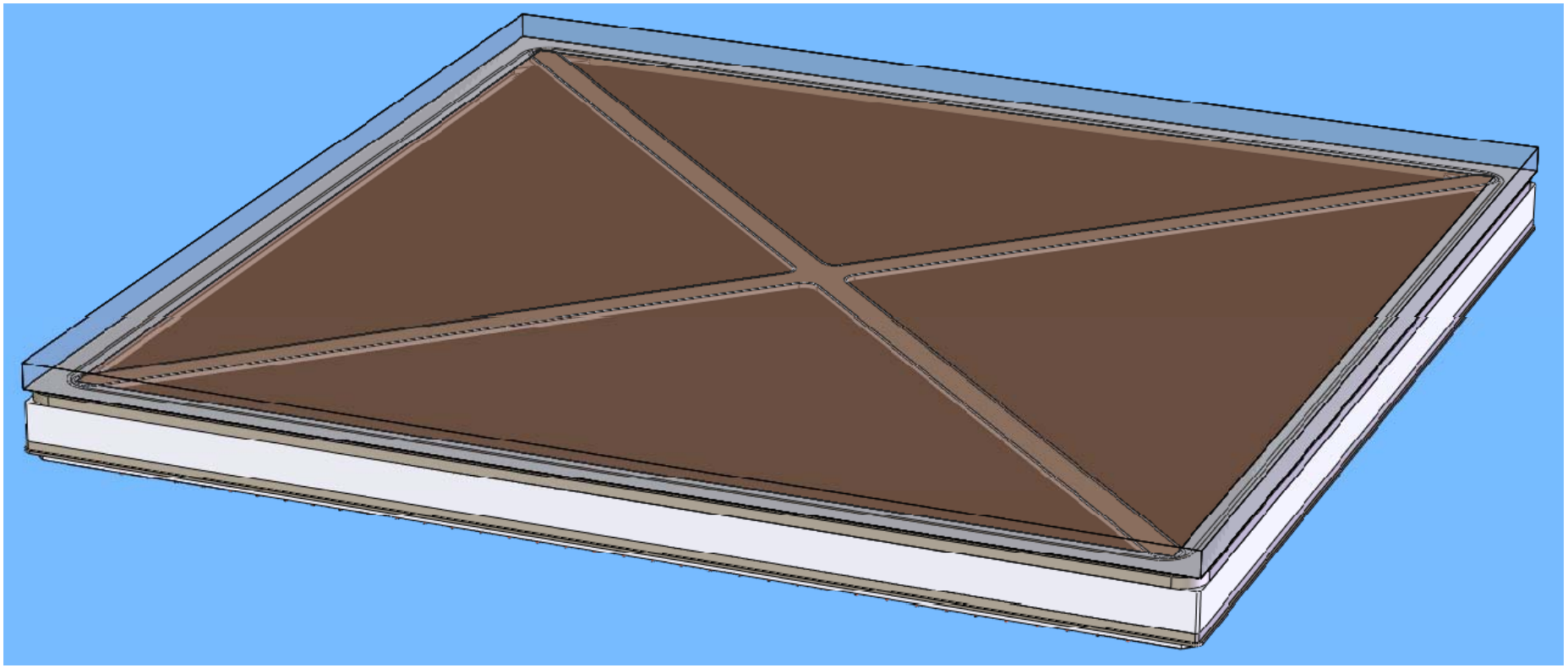


Gary S. Varner
University of Hawai'i
LAPPD Collaboration Meeting
ANL December 10, 2011

8” Ceramic PMT @ SSL

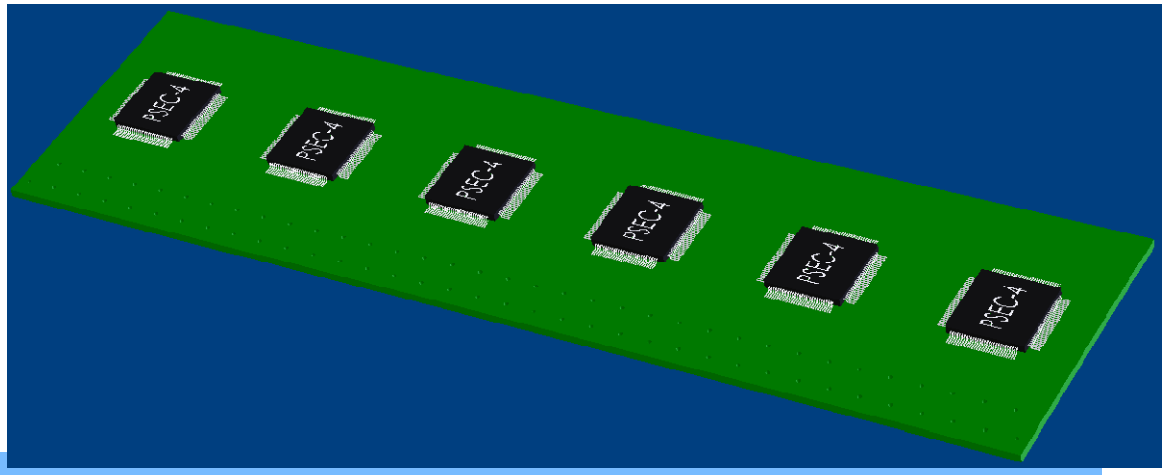
- Baseline (strip-line to outside) design:
  1. PSEC ASIC
  2. Stripline readout
  3. Digital / Central cards

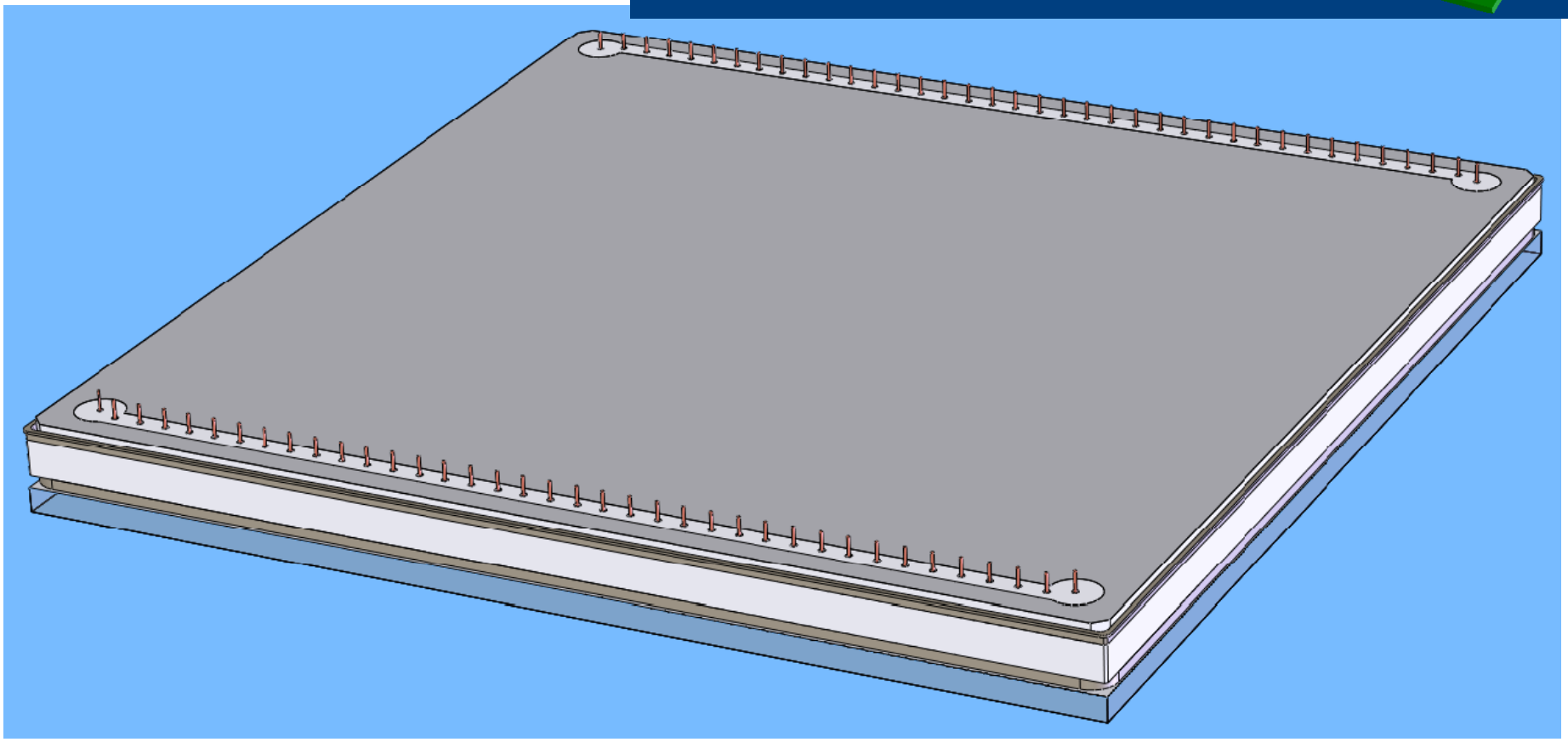
- First fully functional articles:



8” Ceramic PMT @ SSL

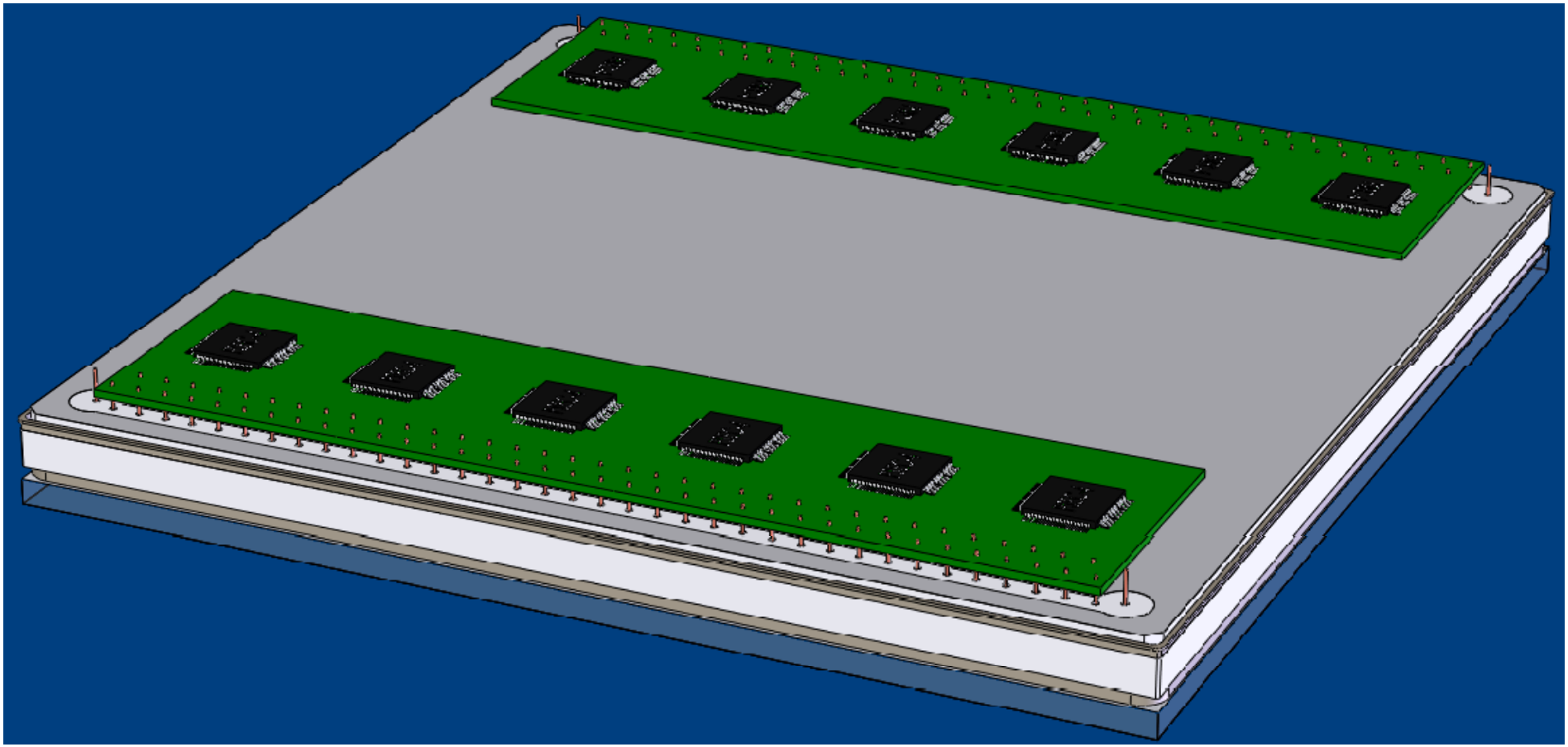
- Ceramic design
  1. Same Analog card ?





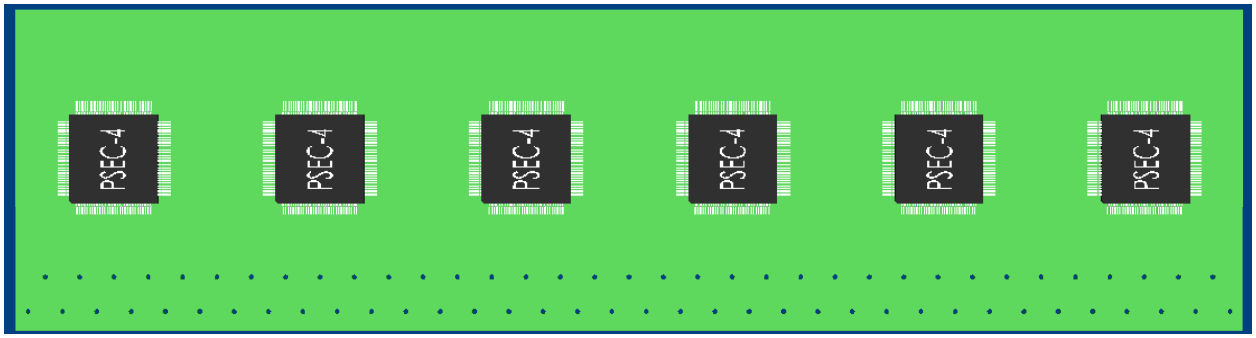
8” Ceramic PMT @ SSL

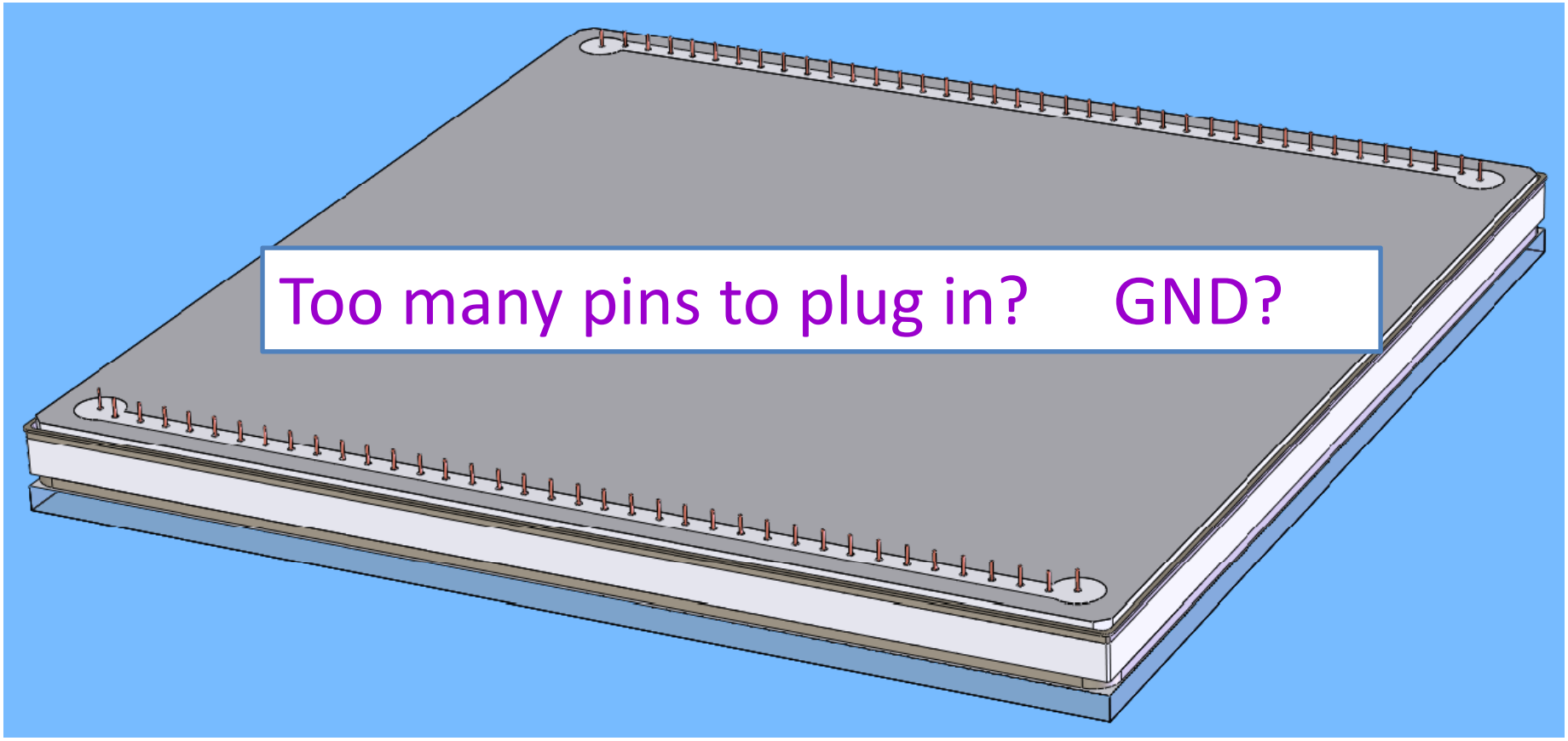
- Ceramic design
  1. Same Analog card ?



8” Ceramic PMT @ SSL

- Ceramic design
  - **1. Different Analog card**
  - **2. Pin readout**

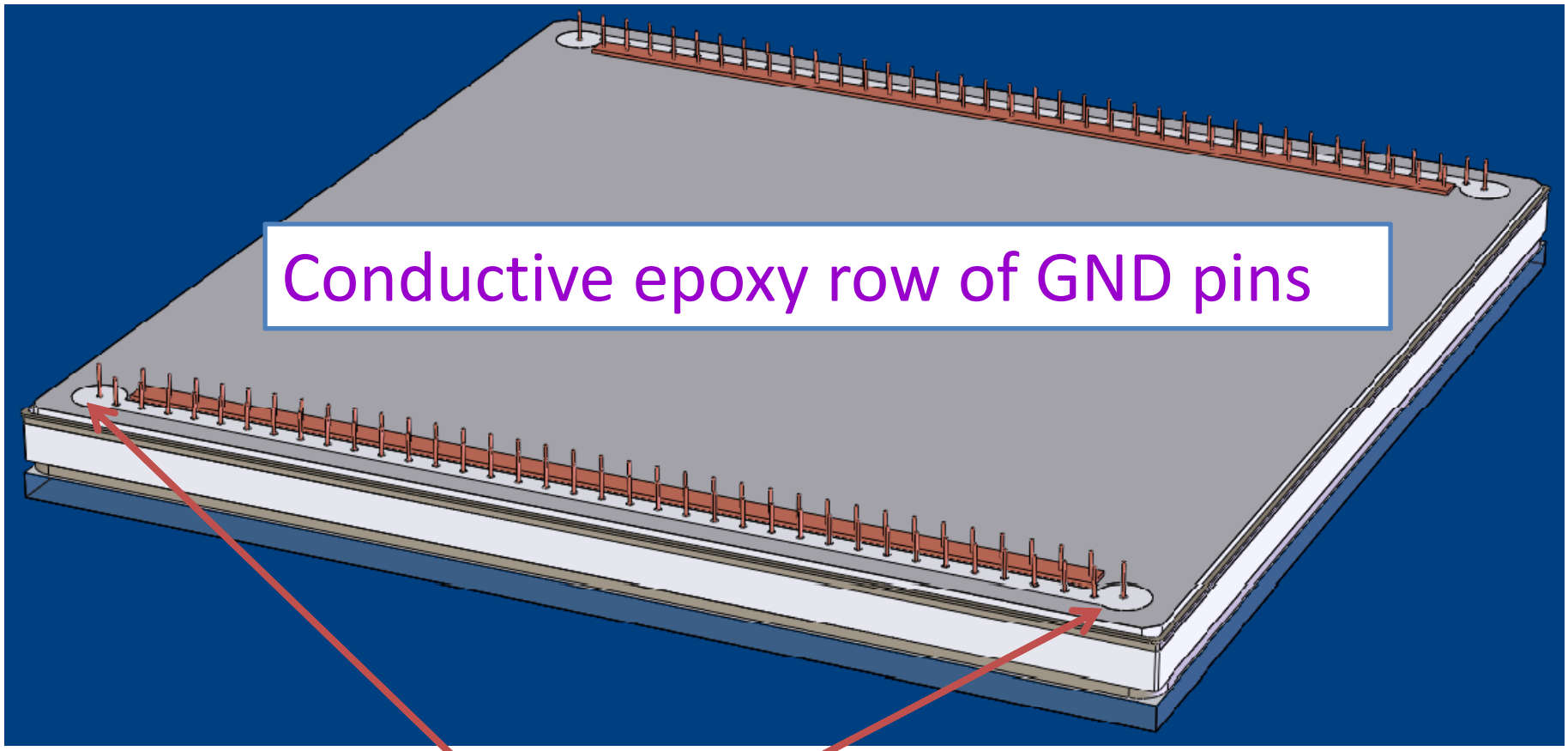




8” Ceramic PMT @ SSL

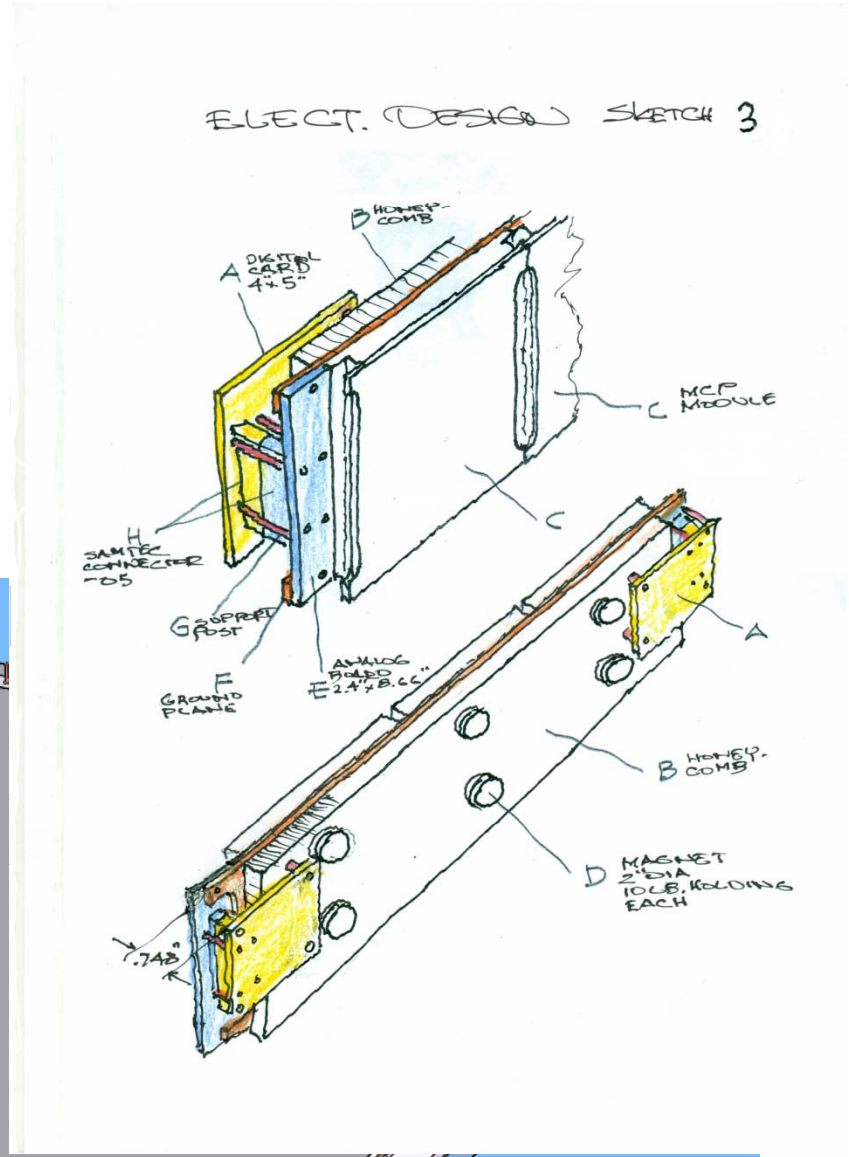
- Ceramic design

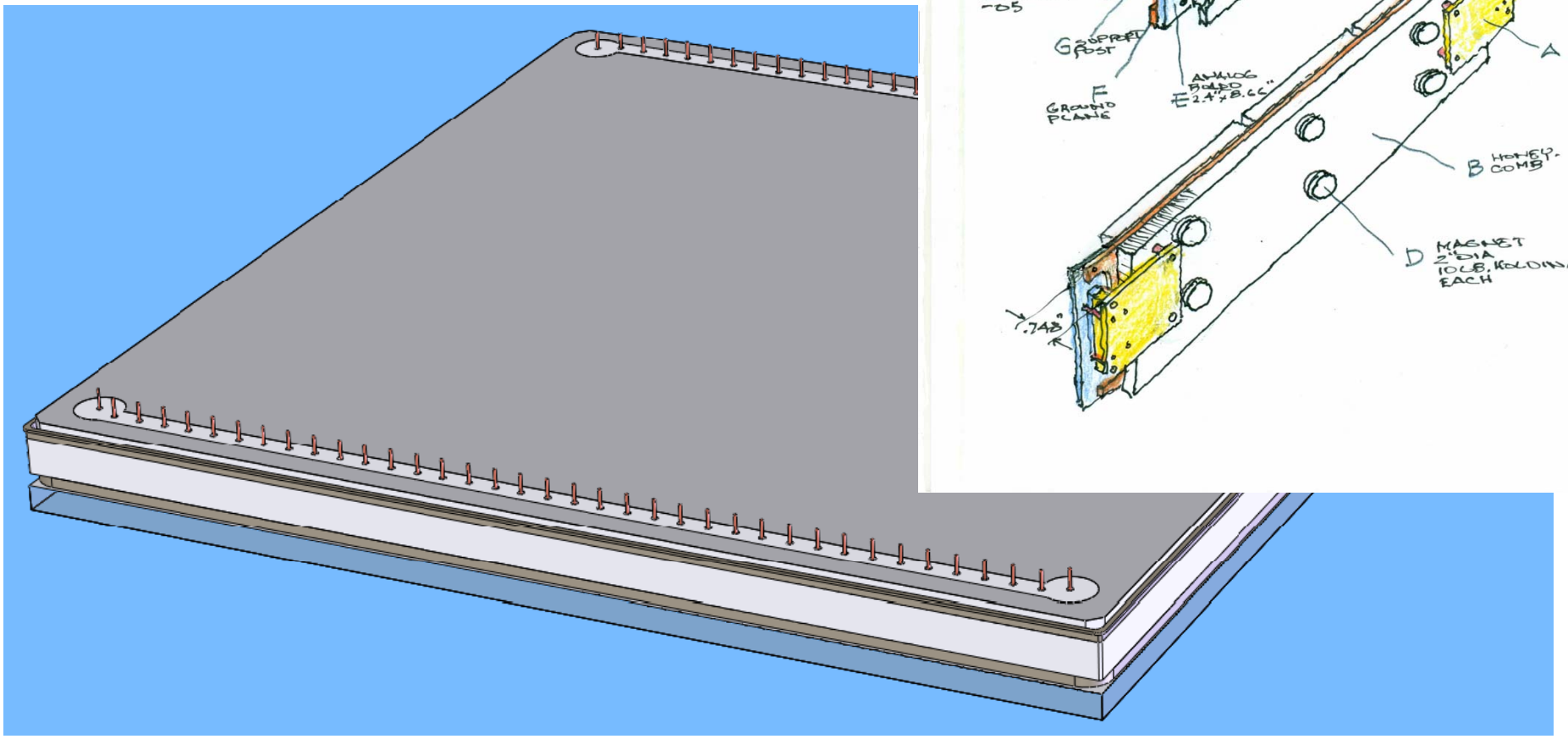
  1. Same Analog card ?



8” Ceramic PMT @ SSL

- Ceramic design
  - **1. Different Analog card**
  - **2. Pin readout**
  - **3. Digital card not mechanically compatible?**

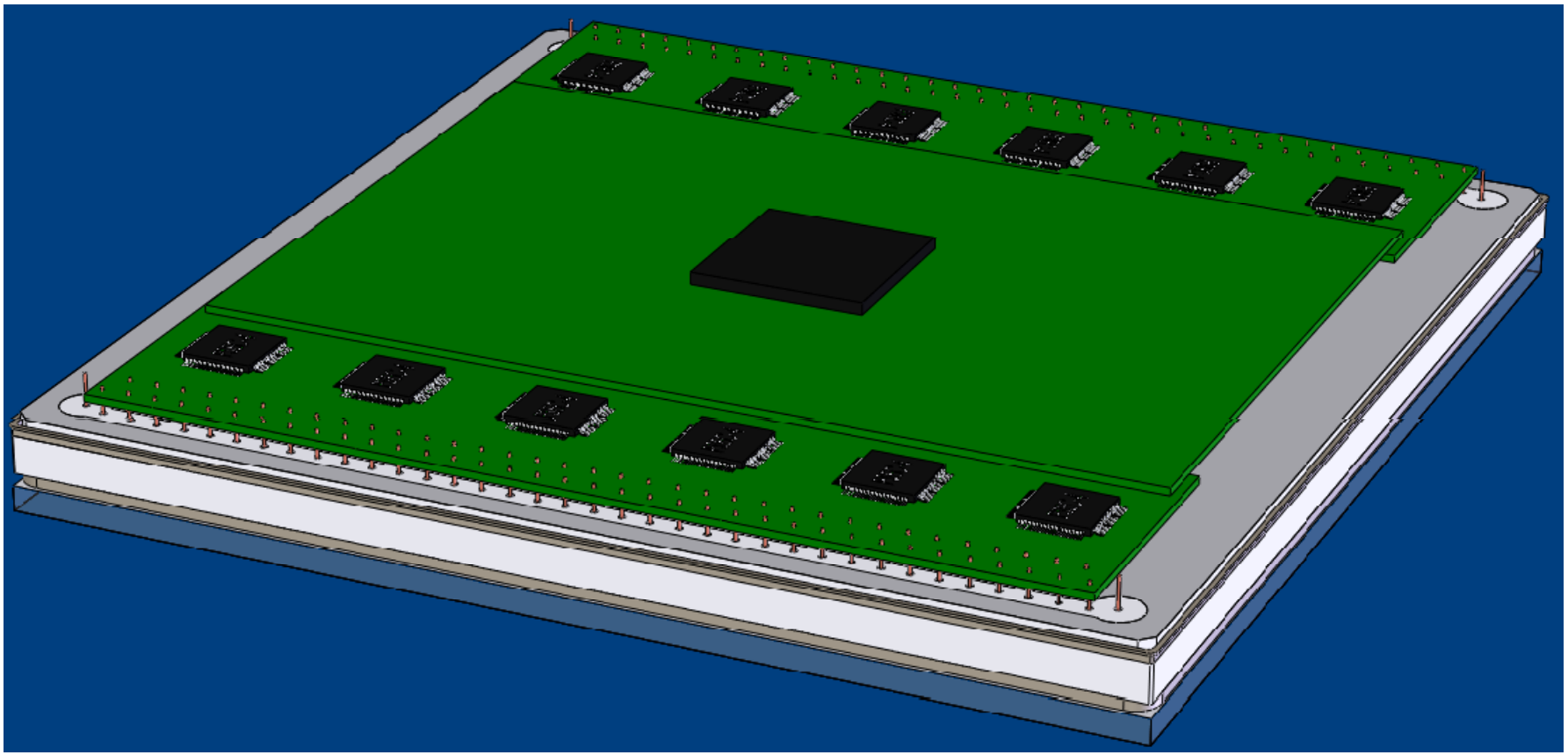




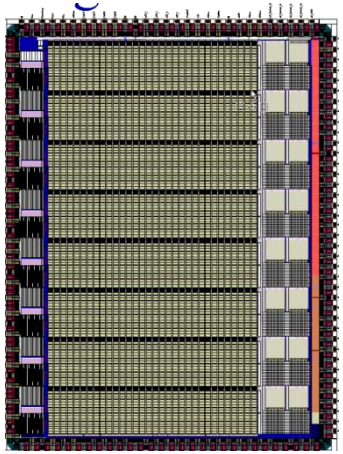
8” Ceramic PMT @ SSL

- Ceramic design
  1. **Different Analog card**
  2. **Pin readout**
  3. **Digital card not mechanically compatible?**

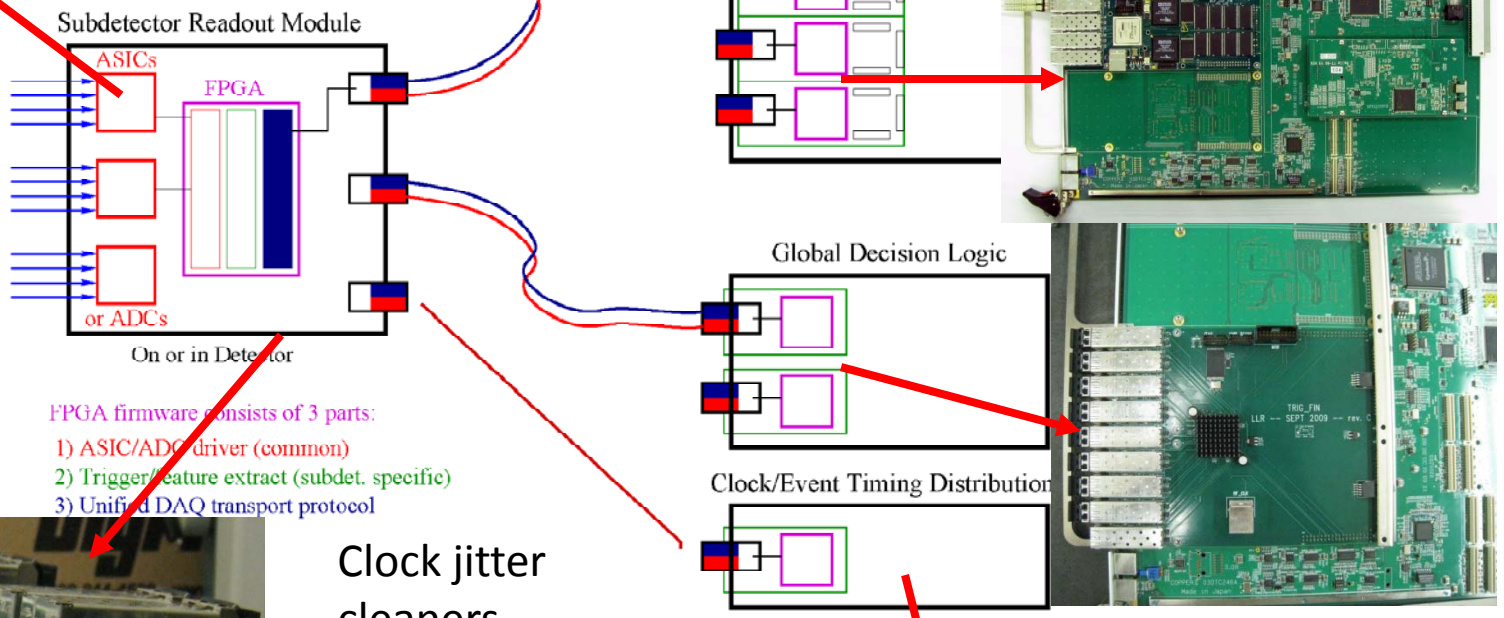
Another digital card ??

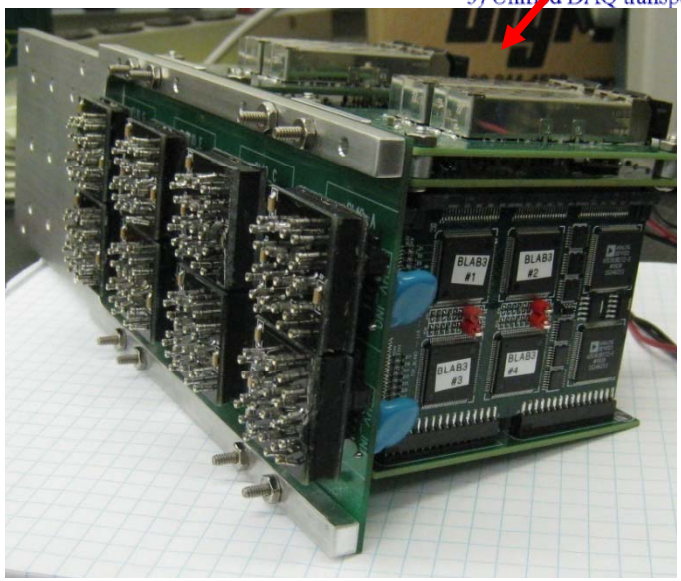


Some relevant experience (Belle II)

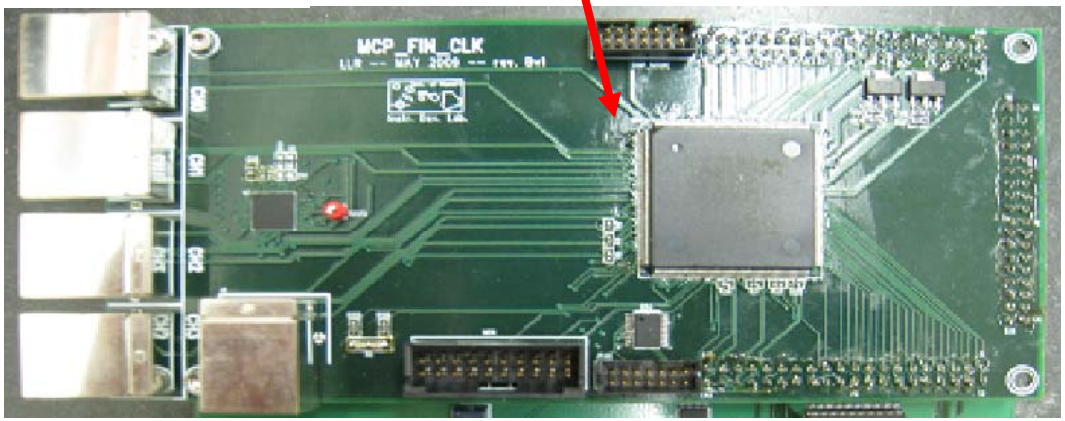


Third generation waveform sampling ASIC



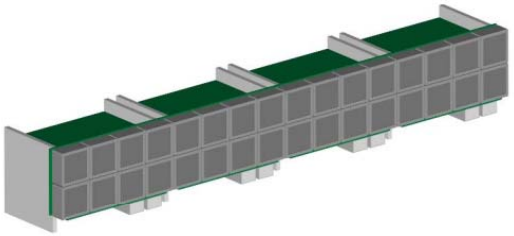


Clock jitter cleaners

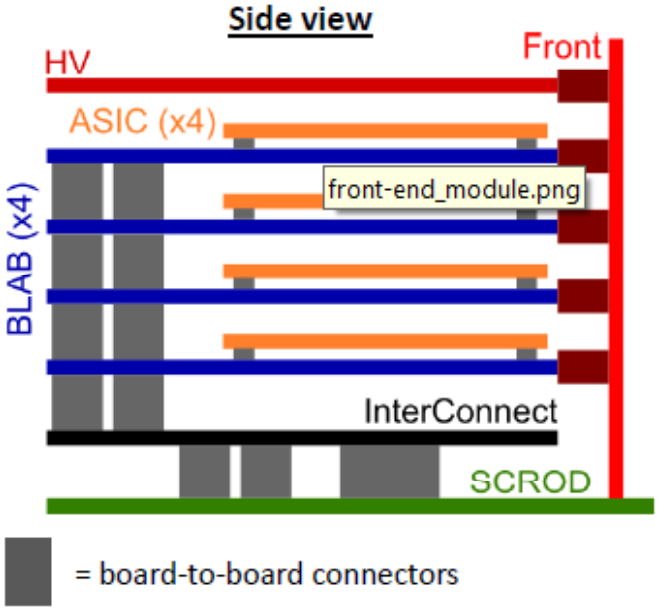


Very compact – Space extreme

32x HPK SL-10
MCP-PMTs = 512 channels



New Front-end Board Stack



Front
- Connects HV board to PMTs
- Connects PMT output to ASIC input

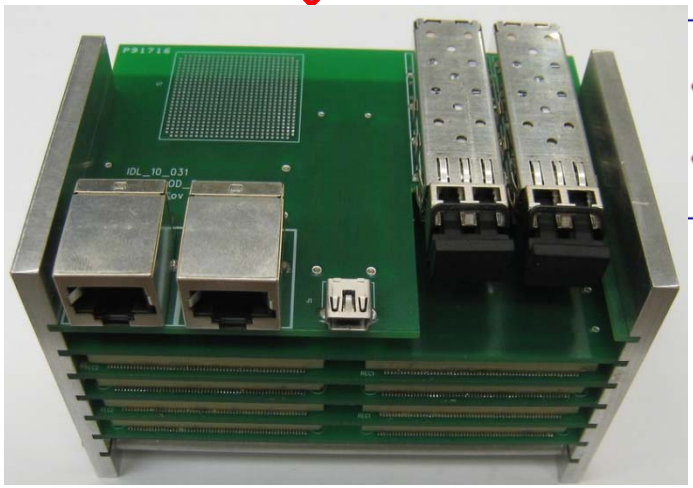
HV
- High voltage components for PMTs
- Cooling for high voltage components

Standard Control, Read-Out, Data (SCROD)
- FPGA (ASIC control)
  - Virtex4, Spartan6
- 2 Fiber transceivers
- 2 RJ45
  - Clock Distribution
  - LVDS (JTAG)
- Mini USB – for easy bench testing

Digitizer Boards (BLAB)
- Carrier card for ASICs
  - 4 ASIC daughter cards per carrier
- ASIC in-situ testing components
  - e.g., pulser for channel checks

ASIC
- 1 BLAB3 per card
- DACs

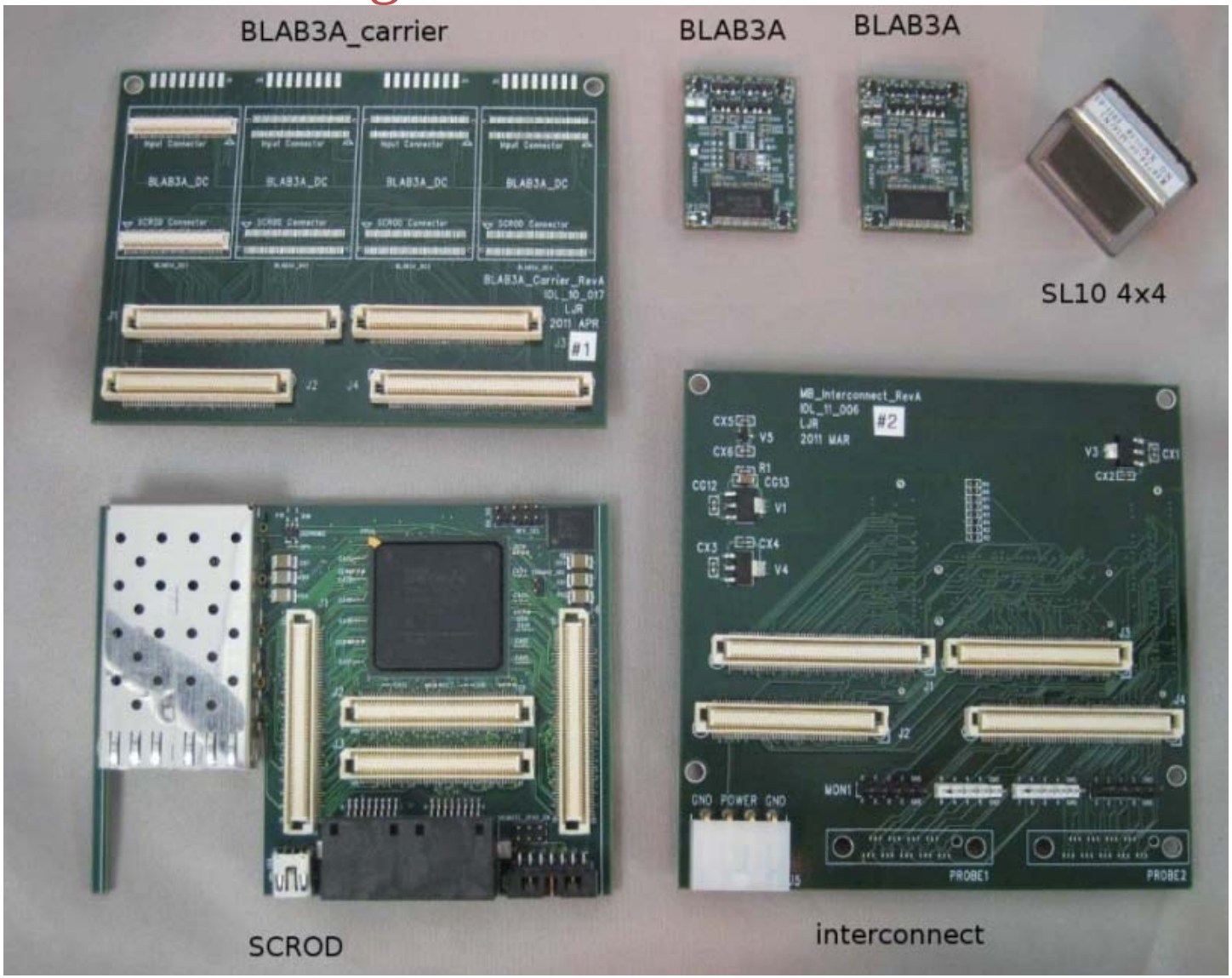
Interconnect Board
- Connects SCROD & BLAB
  -Layout of connectors are forced to be unique because of size constraints
- Power regulation/distribution



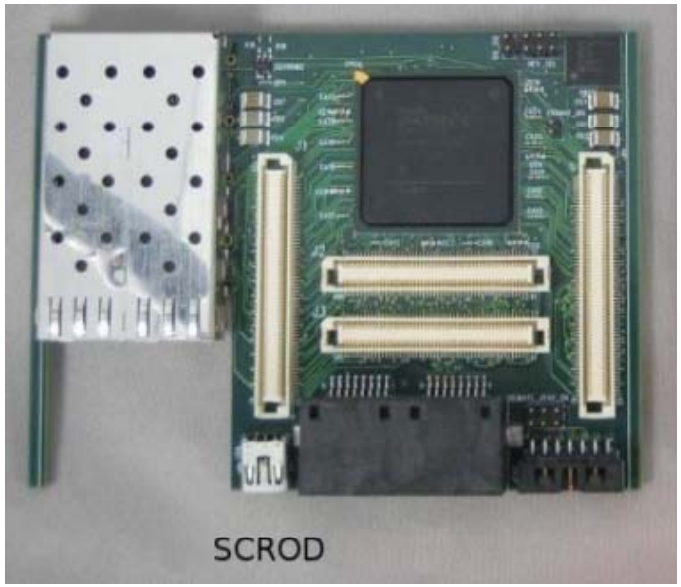
Must fit in very tight space –
addressing some of these issues

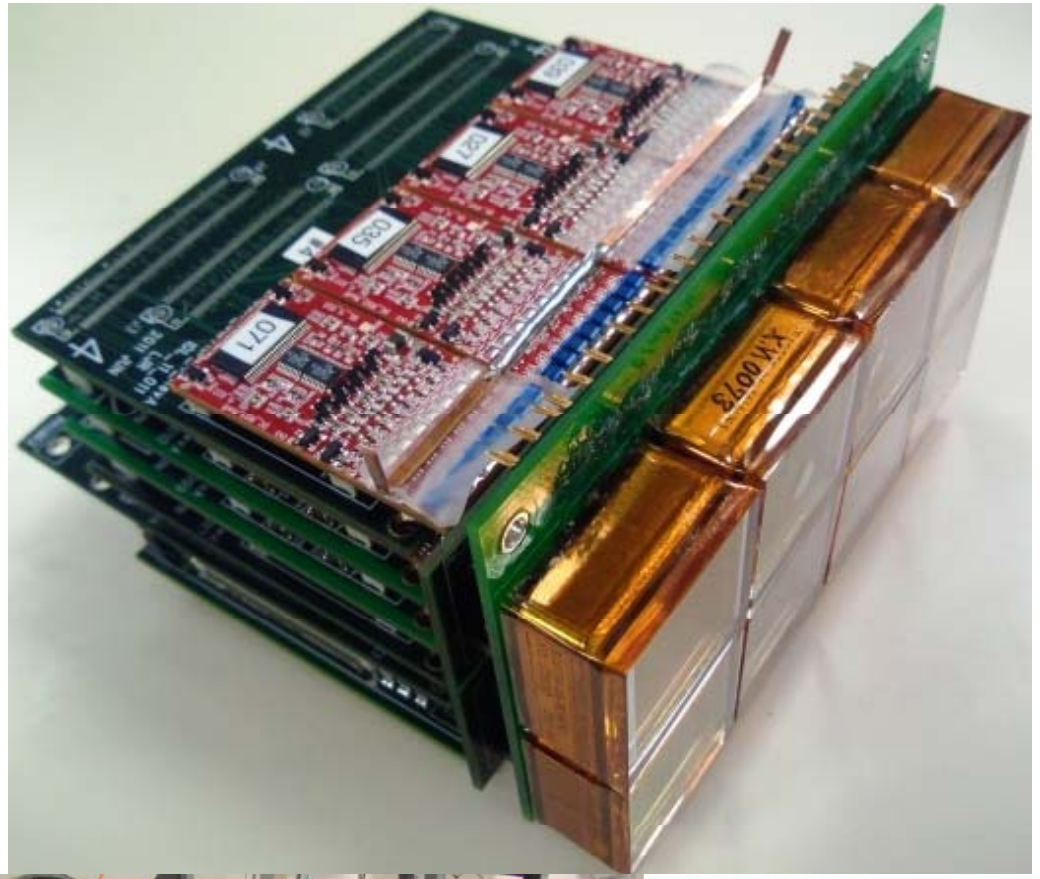
8” Ceramic PMT @ SSL

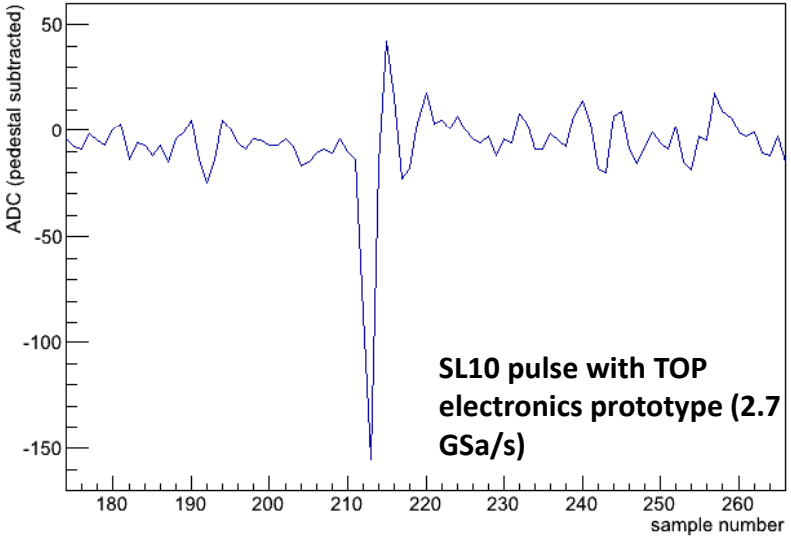
- Not another digital card ?!

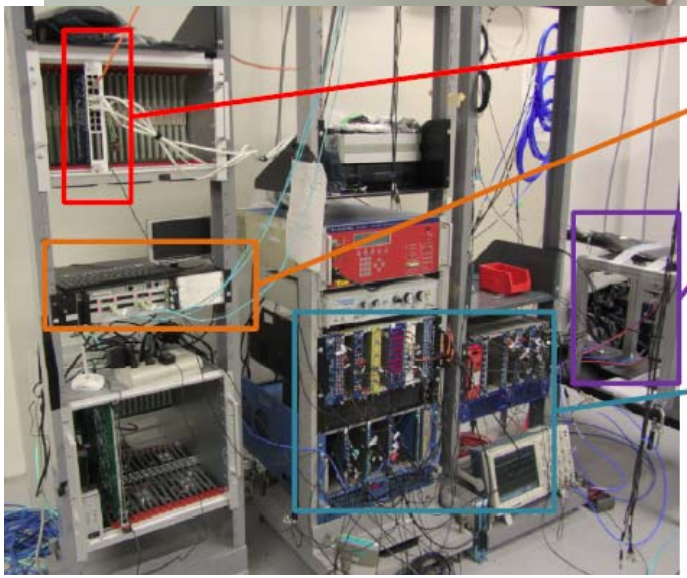


Readout “board stack”



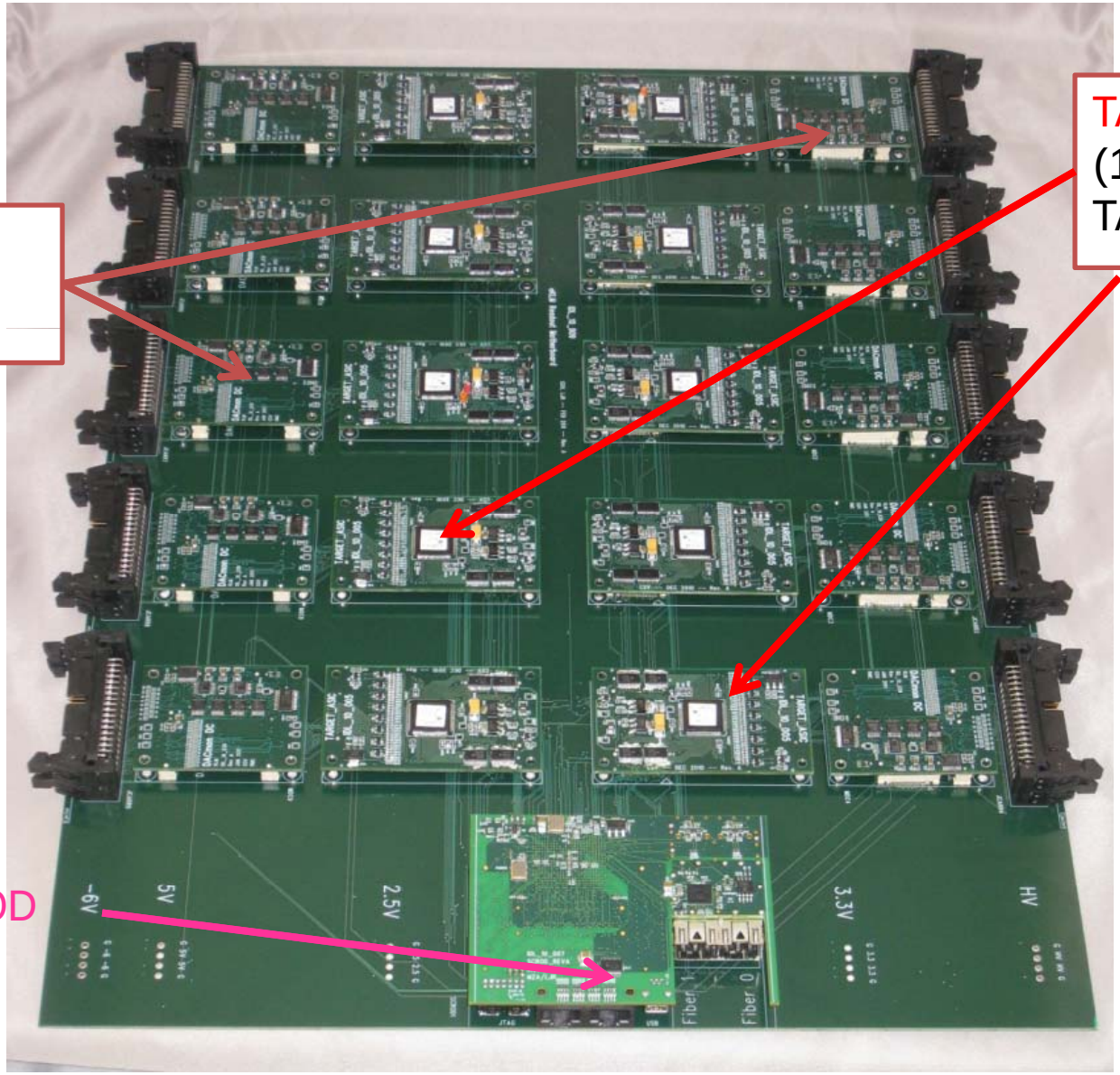




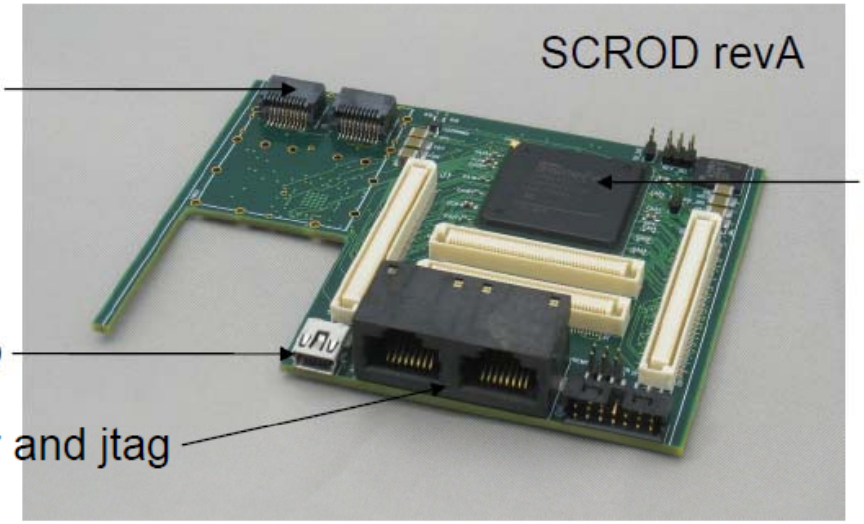


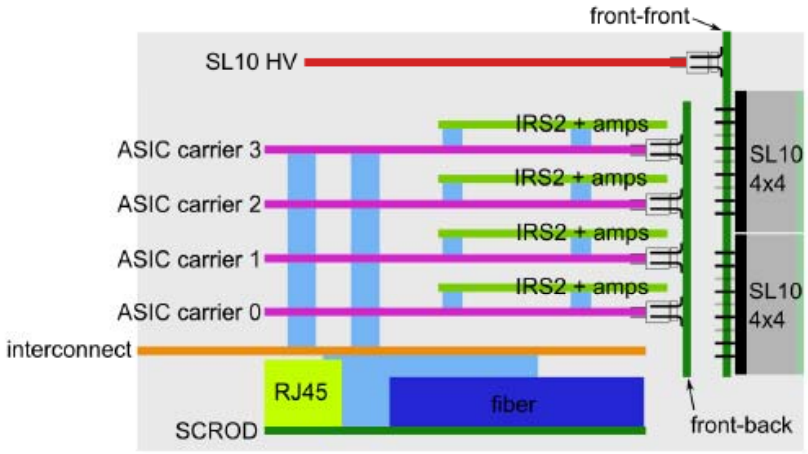
Another example

Different “interface” board

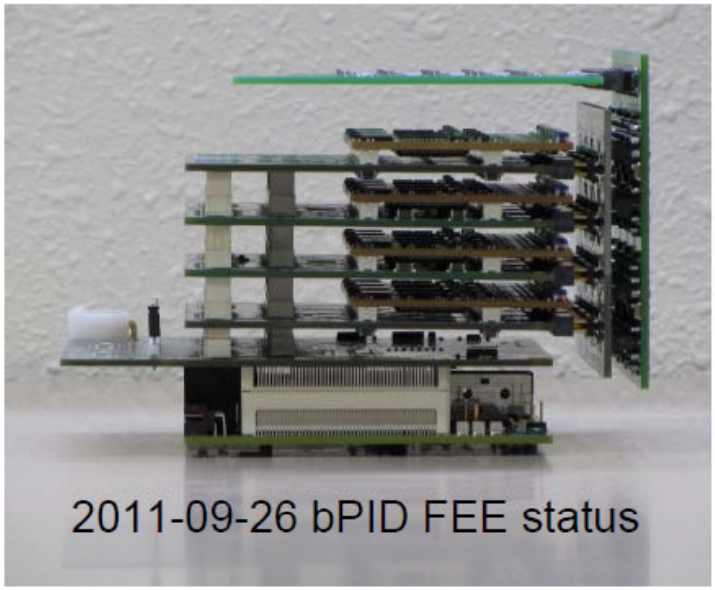


SCROD and board-stack



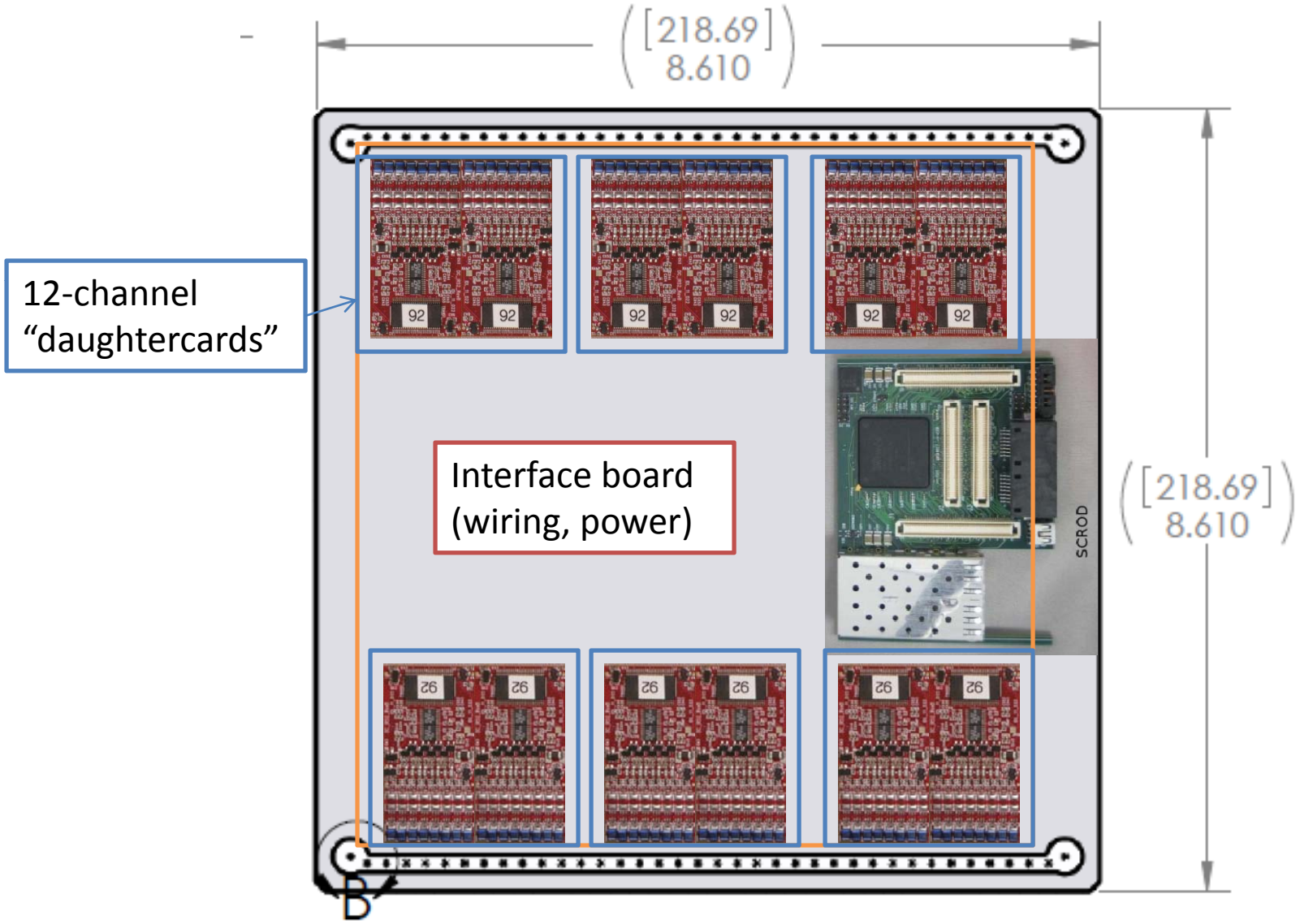


single bPID FEE “board-stack” module
(2011 beam-test version)



One option

Different “interface” board



Readout ASIC Specifications

>= 256	samples/chan
6-8	channels PSEC/IRS ASIC
1	pC nominal
?	pulse height spread?
USB2.0	readout (fiber option)
1-10	GSa/s
1	trigger out per channel?
???	us to read all samples
0.1 - 100	kHz sustained readout (multibuffer?)

- Into 50Ω
  - ~1mV
  - Need gain → SNR of >= 40:1 (40mV on 1mV RMS noise)

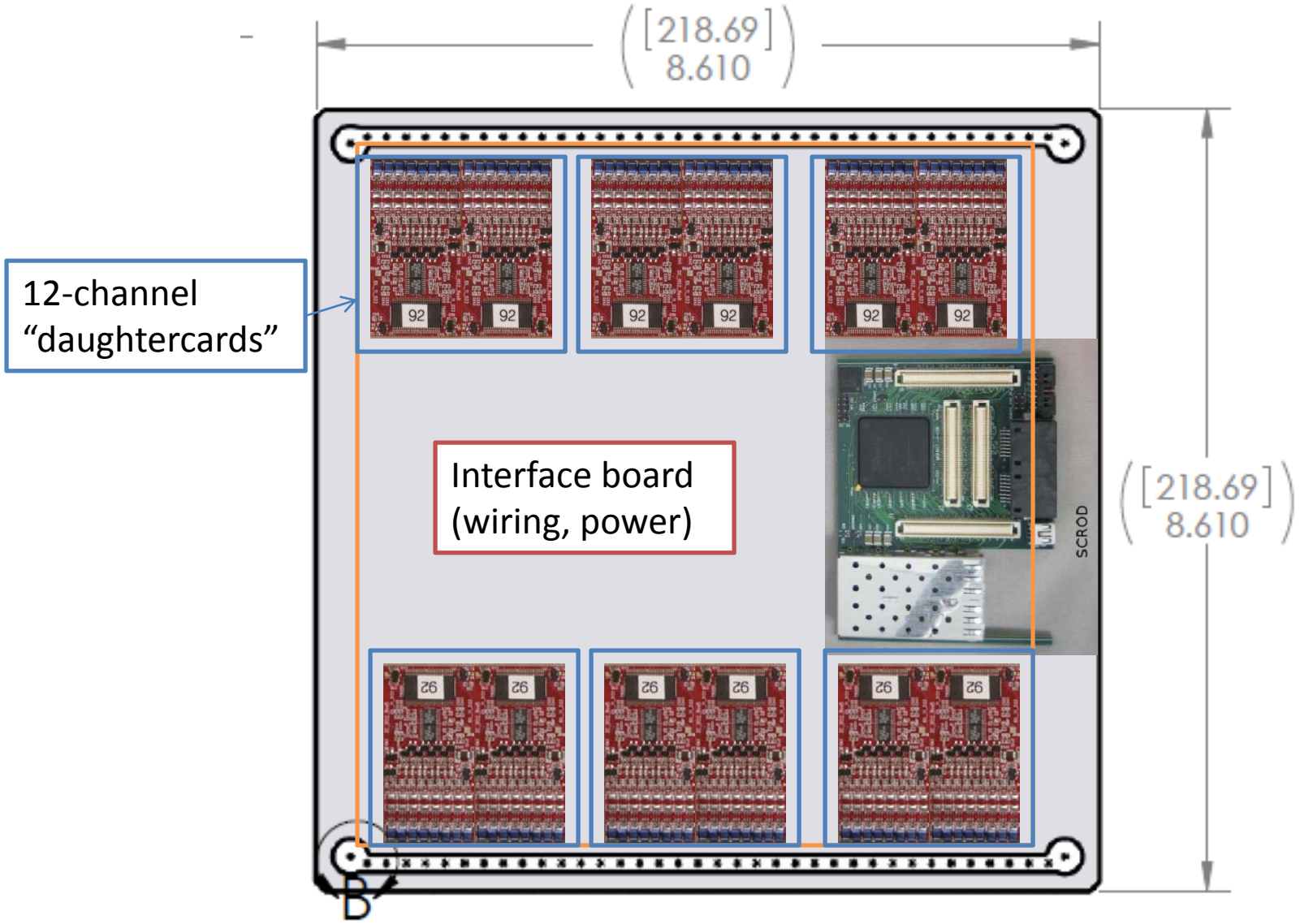
Now a variety of WFS ASIC options…

ASIC	Amplification?	# chan	Depth/chan	Sampling [GSa/s]	Vendor	Size [nm]	Ext ADC?
DRS4	no.	8	1024	1-5	IBM	250	yes.
SAM	no.	2	1024	1-3	AMS	350	yes.
IRS2/IRS3	no.	8	32536	1-4	TSMC	250	no.
BLAB3A	yes.	8	32536	1-4	TSMC	250	no.
TARGET	no.	16	4192	1-2.5	TSMC	250	no.
TARGET2	yes.	16	16384	1-2.5	TSMC	250	no.
TARGET3	no.	16	16384	1-2.5	TSMC	250	no.
PSEC3	no.	4	256	1-16	IBM	130	no.
PSEC4	no.	6	256	1-16	IBM	130	no.

➔ **Success of PSEC3: proof-of-concept of moving toward smaller feature sizes.**

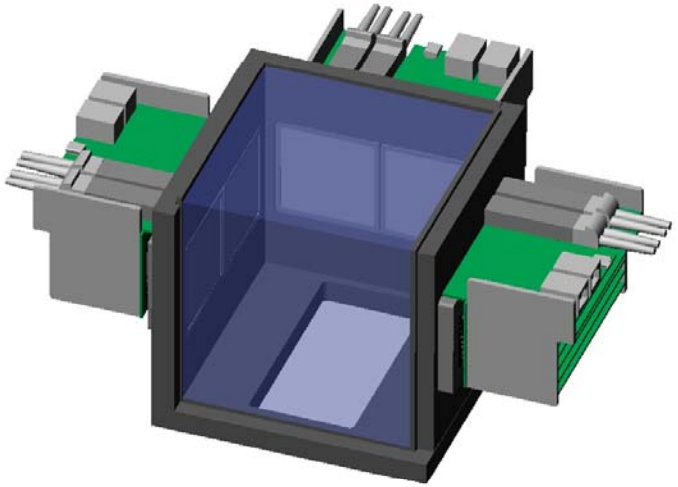
- Next DRS plans to use 110nm; next SAM plans to use 180 nm.

Baseline options:
2x PSEC4, 2x IRS3, 1x TARGET per DC

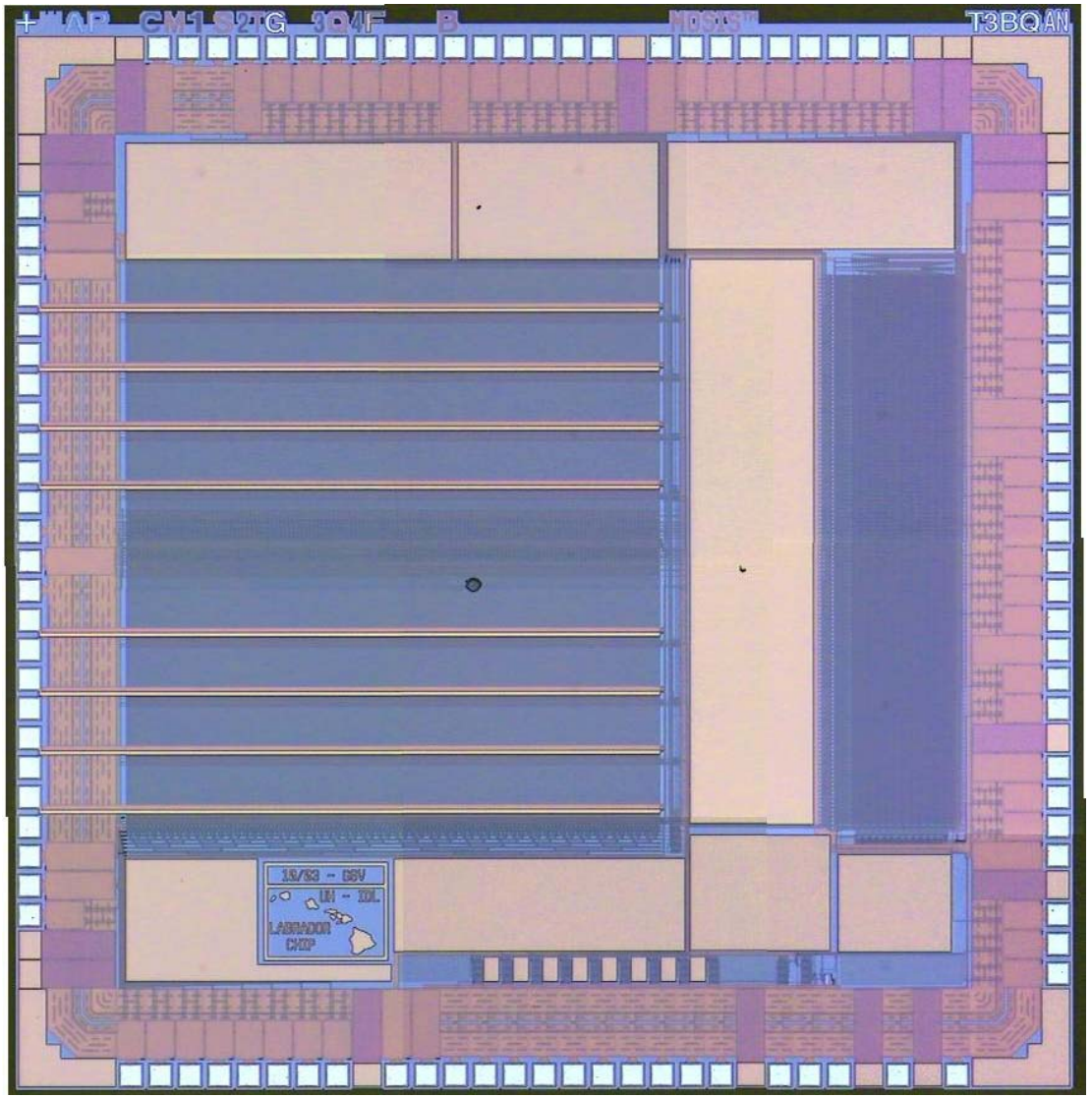


Design Issues

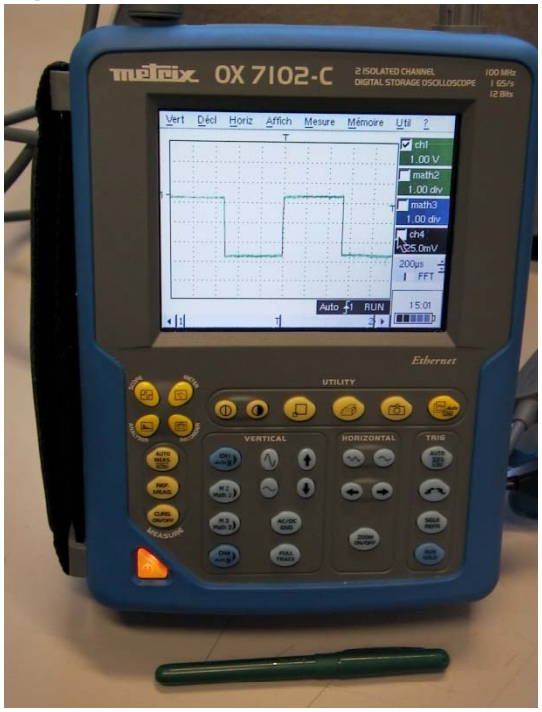
- Want something on timescale of demonstration tube
  - Use existing ASICs
  - Timing performance of 20-30ps OK?
- Readout via SCROD
  - Leverage existing back-end/firmware
  - Higher event rate possible
  - Deeper (continuous) sampling?
  - Faster, sparsified readout
  - Calibration
- Longer term
  - Digital/Central card specific to LAPPD
  - “up front” sparsification best

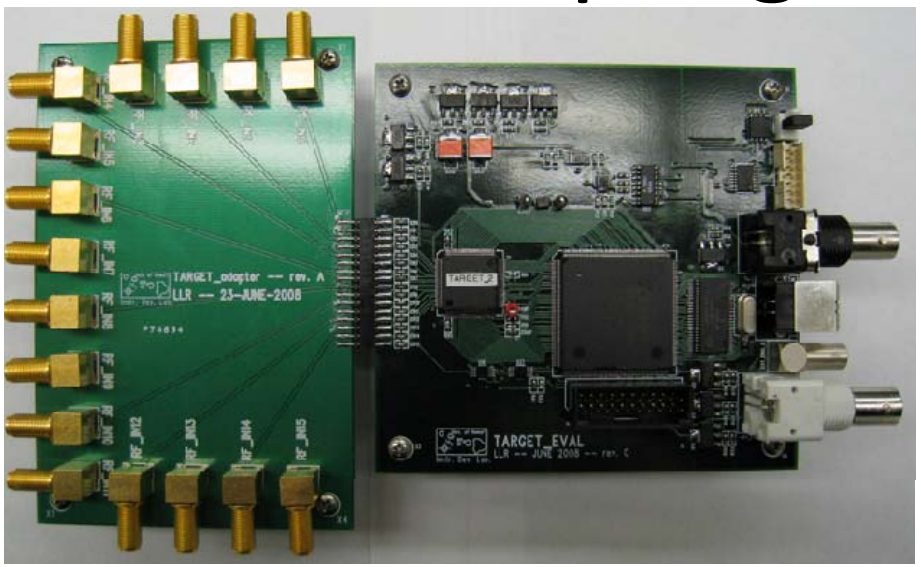


Back-up slides



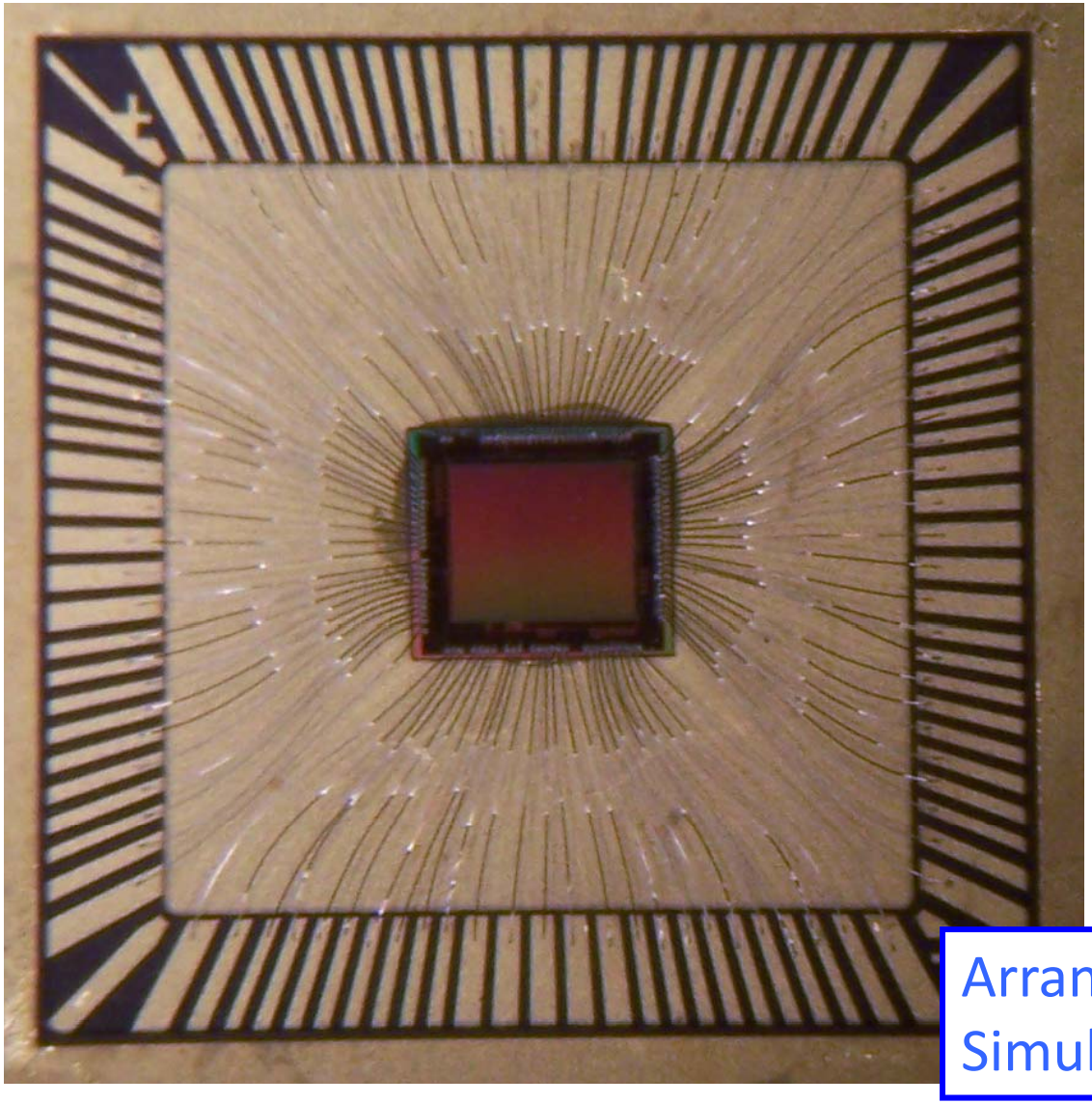
Easy access to Waveform sampling





	WFS ASIC	Commercial
Sampling speed	0.1-6 GSa/s	3 GSa/s
Bits/ENOBs	16/9-13+	8/7.4
Power/Chan.	<= 0.05W	Few W
Cost/Ch.	< $10 (vol)	> 100$

Deeper storage: Buffered LABRADOR (BLAB1) ASIC



3mm x 2.8mm, TSMC 0.25um

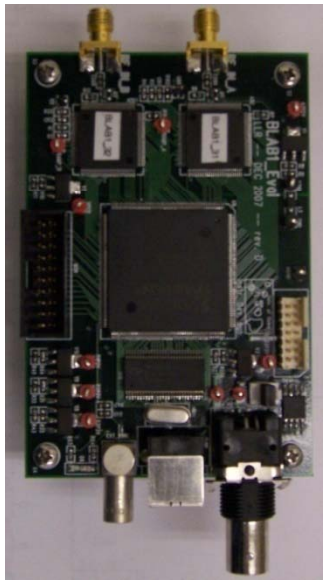
- Single channel
- 64k samples deep, same SCA technique as LAB, no ripple pointer
- Multi-MSa/s to Multi-GSa/s
- 12-64us to form Global trigger

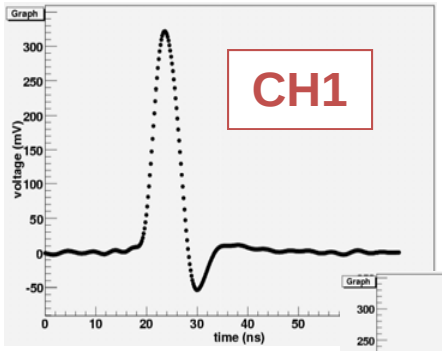
Arranged as 128 x 512 samples
Simultaneous Write/Read

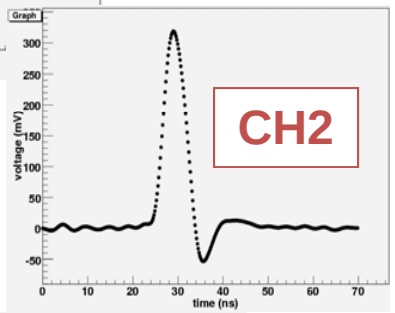
BLAB1 High speed Waveform sampling

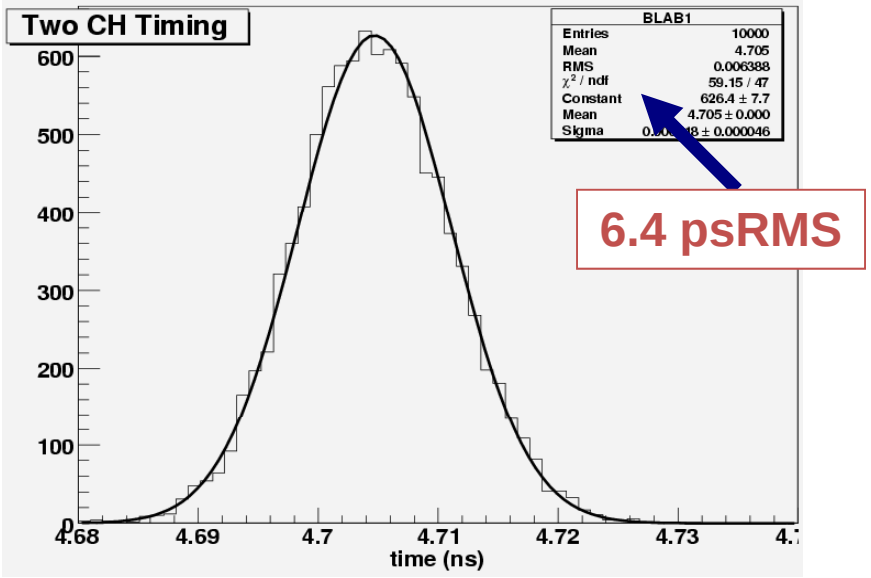
- Comparable performance to best CFD + HPTDC
- MUCH lower power, no need for huge cable plant!
- Using full samples reduces the impact of noise
- Photodetector limited

NIM **A602** (2009) 438

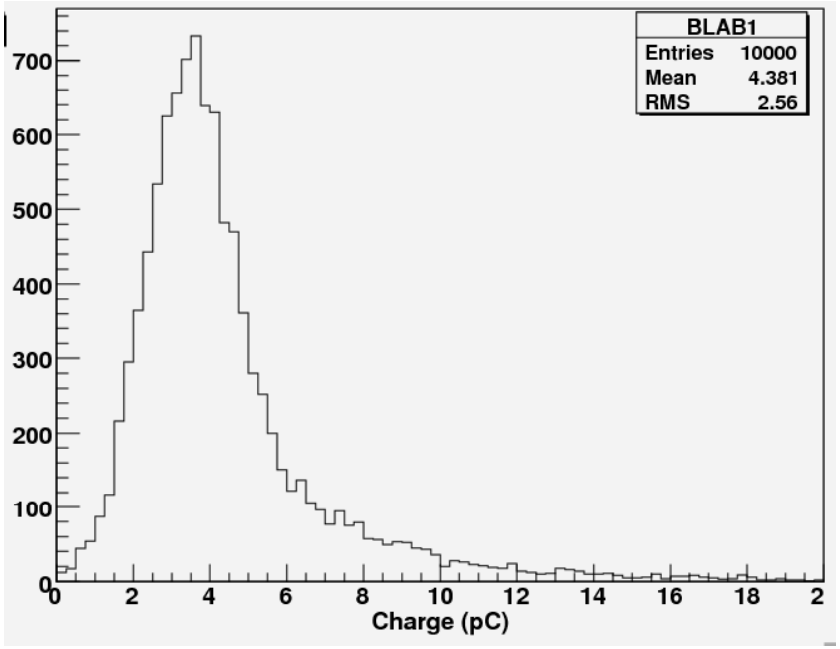


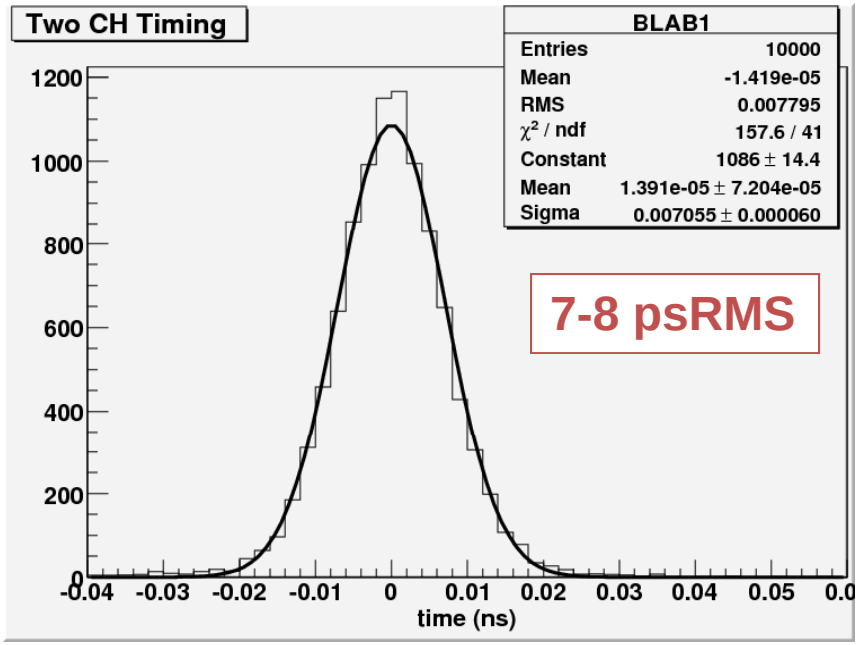






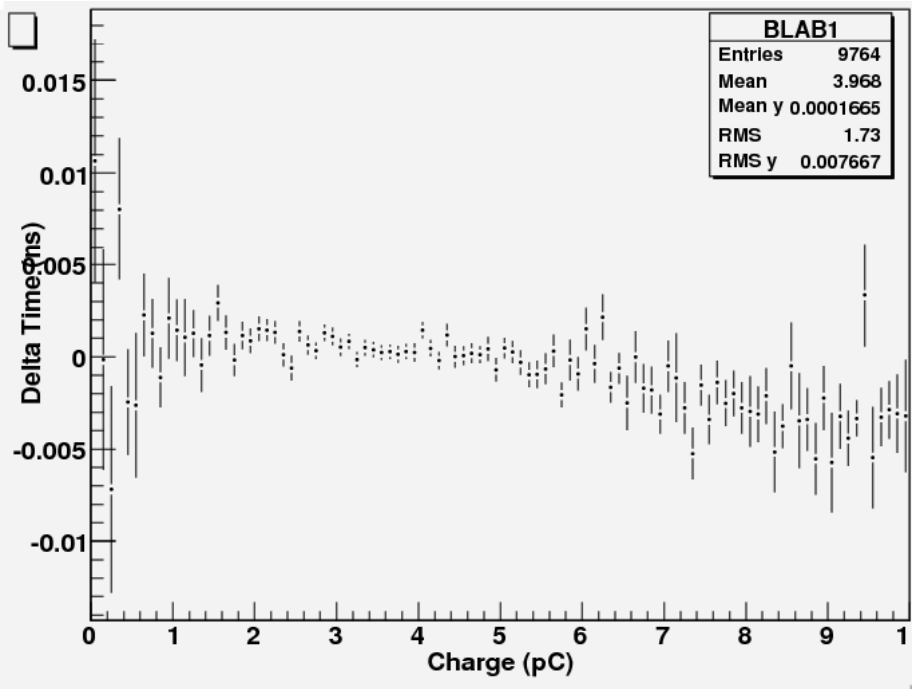
Real MCP-PMT Signals (with BLAB2)





7-8 psRMS

Residual Time Walk



Rather robust for amplitude invariant signals,
TOF still hard, but can shape extract

Ice Radio Sampler (IRS) / Buffered LABRADOR 3 (BLAB3) Specifications

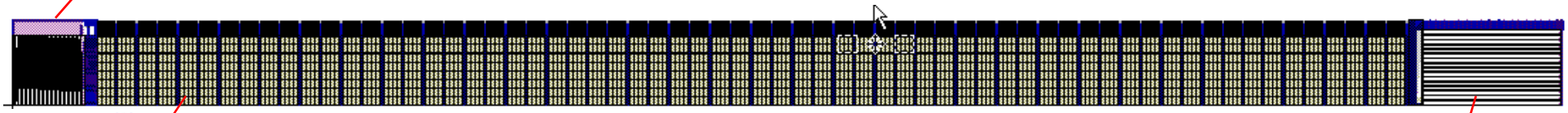
32768	samples/chan (8-32us trig latency)
8	channels/IRS ASIC
8	Trigger channels
~9	bits resolution (12-bits logging)
64	samples convert window (~16-64ns)
1-4	GSa/s
1	word (RAM) chan, sample readout
16	us to read all samples
100's	Hz sustained readout (multibuffer)

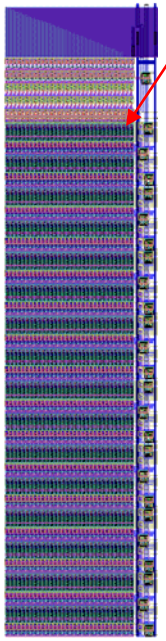
- Difference between IRS/BLAB
  - BLAB has input amplifier
  - IRS doesn't really use internal trigger capability

IRS/BLAB3
Single Channel

- Sampling: 128 (2x 64) separate transfer lanes

Recording in one set 64, transferring other
("ping-pong" → "2 stage sampling")



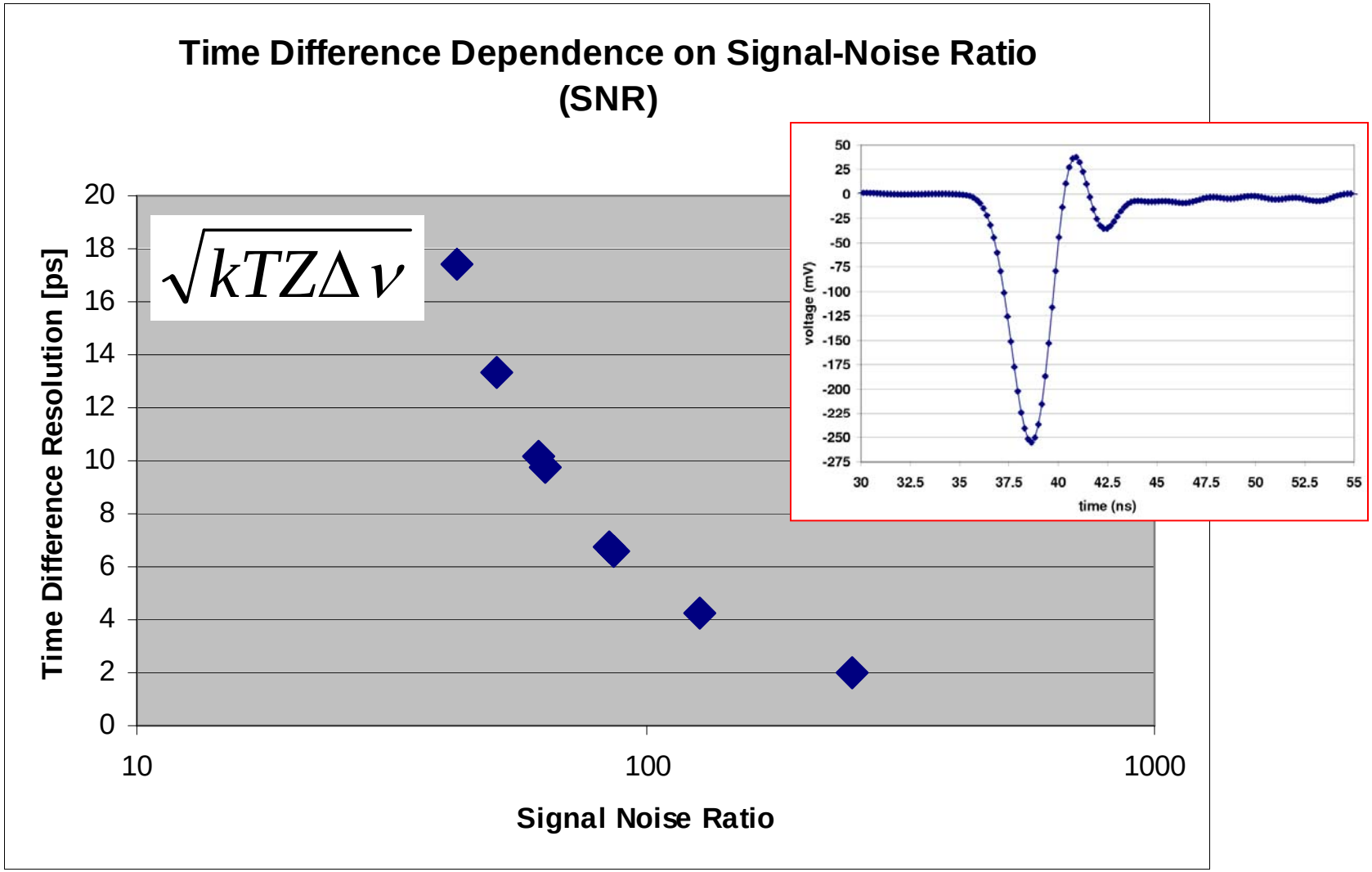


- Storage: 64 x 512 (512 = 8 * 64)

- Wilkinson (32x2): 64 conv/channel

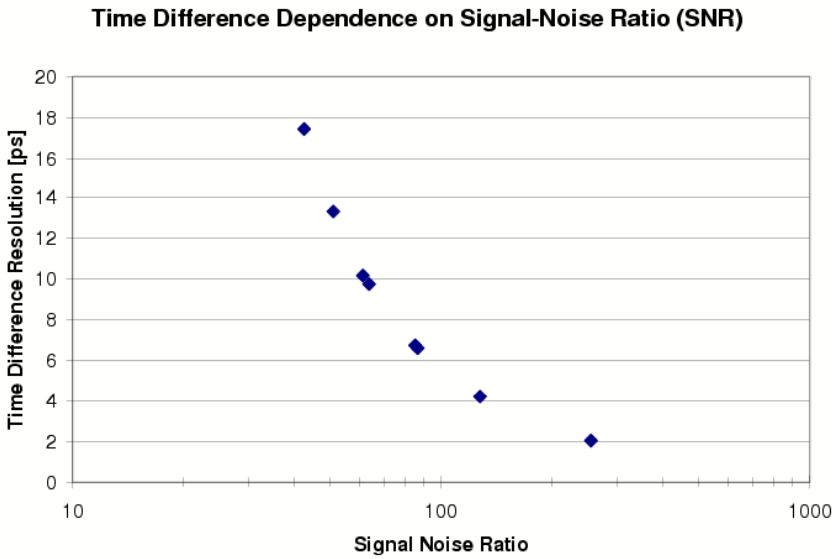
Simulated Performance vs. SNR

300MHz ABW, 5.9GSa/s



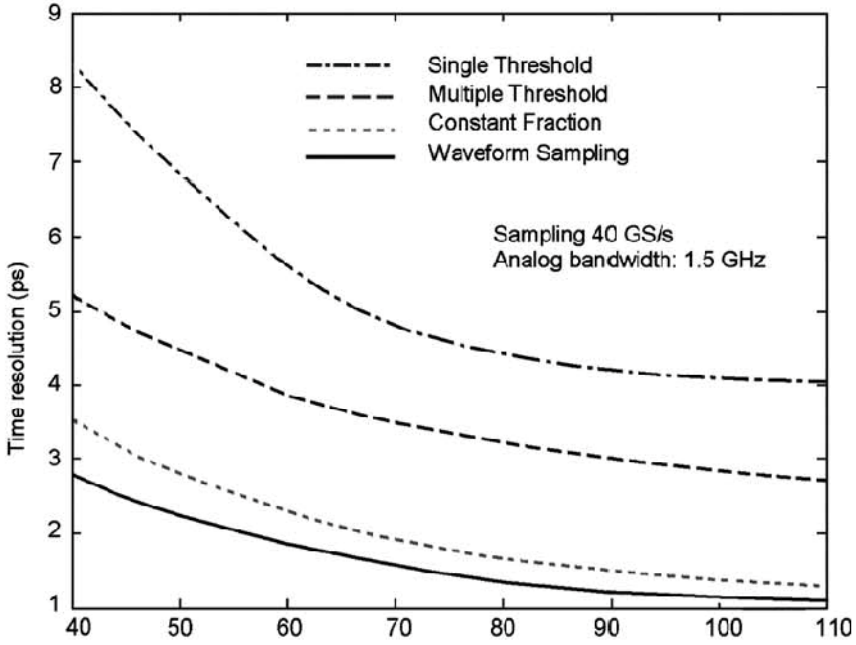
Front-end Electronics studies

1GHz analog bandwidth, 5GSa/s



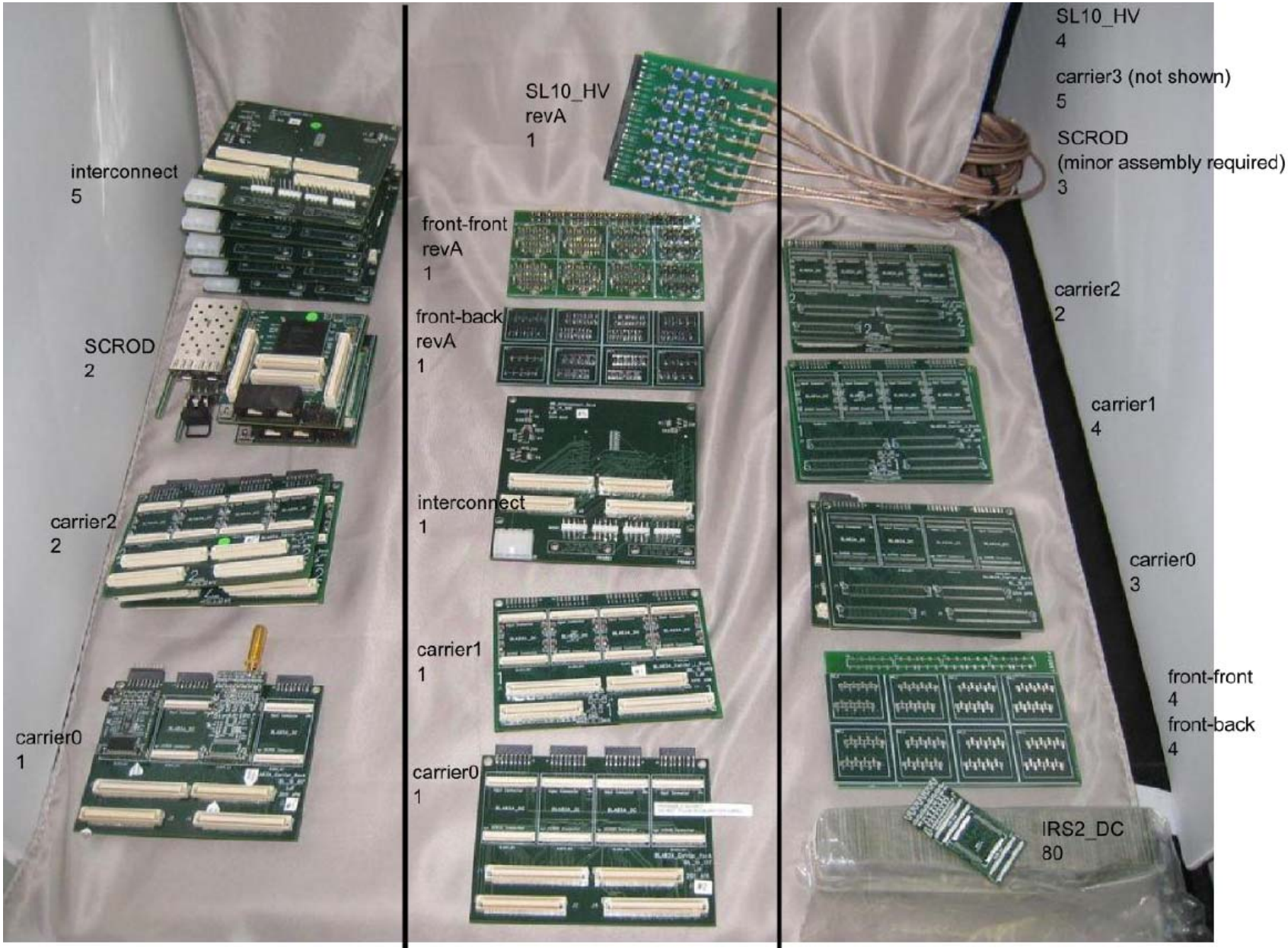
G. Varner and L. Ruckman
NIM A**602 (2009) 438-445**.

Simulation includes detector response

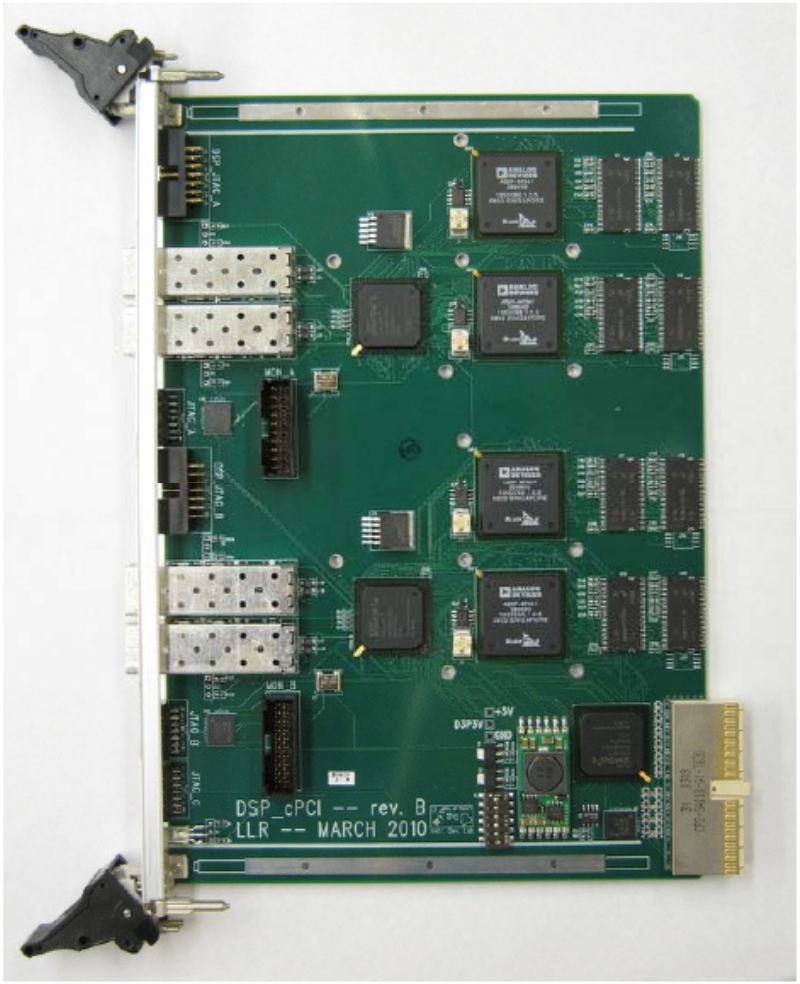


J-F Genat, G. Varner, F. Tang, H. Frisch
NIM A**607 (2009) 387-393**.

Front-end Assembly Status



bPID back-end electronics status



DSP_cPCI

firmware tasks (Xin Gao, Serge Negrashov, Kurtis Nishimura, Matt Andrew):

- Aurora/RocketIO data in from fiber optics
- FPGA-FPGA interface
- PCI interface
- DSP interface (skipping this for now)

software tasks (Serge Negrashov & Andrew Wong):

- linux kernel driver
- "userland" library
- "userland" test program
  - "userland" program to raw data dump-to-disk for cosmic run / actual beam-test

overall integration, front-end to back-end:

- only 94% raw data fidelity
  - still have some bugs to work out

References

- PSI activities (DRS)
  - IEEE/NSS 2008, TIPP09
  - **http://midas.psi.ch/drs**
- DAPNIA activities
  - MATDAQ: *IEEE TNS 52-6:2853-2860,2005 / Patent WO022315*
  - SAM; *NIM **A567** (2006) 21-26.*
- Hawaii activities
  - STRAW: Proc. SPIE 4858-31, 2003.
  - PRO: JINST, Vol. **3**, P12003 (2008).
  - LABRADOR: NIM **A583** (2007) 447-460.
  - BLAB: NIM **A591** (2008) 534-545; NIM **A602** (2009) 438-445.
  - STURM: EPAC08-TUOCM02, June, 2008.