**TEST BOARD** 1 for ps\_TDC\_01

* Primarily D.C. tests using 10 packaged chips (120 pins) from MOSIS. Package chip size is roughly 1 x 1 sq. inch.
* Goals:
  + Make sure a full test card is a good investment
  + Get some preliminary results

**DESIGN**

* Test Board Size: TBD
* Number of layers: TBD
* Number of pins: 16
* Number of potentiometers: 8
* Controllable inputs on board (19):
  + *Chip power* (2): vdd, gnd
  + *Ramp* (2): Ibias\_rp (current to ramp), Rp (enable ramp cap)
  + *Comparator* (test structure, 3): Ibias\_comp (current to comp), comp\_p (V+), comp\_n (V-)
  + *Ring Oscillator* (test, 3): VG2N, VG2P (RO voltage controls), Clear\_test (clear RO counter)
  + *Sampling Cell* (test, 6): Vpol\_cell, In\_test, Biasl\_test, Trig\_test, Ctrl\_rd\_test, Write Test
    - note: Biasl\_test of cell test structure shorted to input return biases (Biasr, Biasl) of channels 0,1,2,3. This allows us to observe power dissipation of 256 sampling cells/channel as a function of bias voltage.
  + *Token* (3) : Clear\_token, Tok\_in (Input), Ck\_rd (Read Clk)
    - note: Ck\_rd is the only AC clock to the board – ideally 40 MHz

---All DC inputs with 1 uF decoupling capacitor from signal to gnd.

**PIN DETAIL**

Direct input pins (using banana jacks): vdd, gnd

**-**Control via voltage pot (5K): In\_test, Biasl\_test, Comp\_p, VG2N, VG2P, Vpol\_cell

-Current control pot (1M): Ibias\_Rp, Ibias\_comp

LEMO input pins: Rp, comp\_n, Trig\_test, Ctrl\_rd\_test, Write\_test, Clear\_token,

Tok\_in, Ck\_rd, Clear\_test

* Output pins on board (5):
  + comp\_out (observe comparator test structure output)
  + 2G\_test\_out (observe RO test structure output /4096)
  + Cext (I/O) (observe internal ramp output – can be used as input too)
  + Token\_out (observe token output)
  + Samp\_out (observe sampling cell test structure output)

---Unused input and output pins on chip grounded

**PIN DETAIL**

LEMO out: comp\_out, 2G\_test\_out, Cext, Token out, Samp\_out

**TESTS** (a general overview)

Low-level

* Turn on chip by slowly raising vdd
  + measure current/power

Intermediate Level

* Determine DC power contributions from various structures
  + power as a function of biases

Higher-level

* Observe function of chip structures (comparator, ramp, token, ring oscillator, sampling cell)