The Factors That Limit Time Resolution in Photodetectors

Dependence on Feature Size

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Outline

- **Basic Notation**

- **Survey of Feature Sizes**

- **How Feature Size Affects Speed – Scaling Laws**

- **Consequences of Deep Submicron Technologies**

- **Practical Considerations**

- **Summary**

Basic Notations & Principles in CMOS Design

- **Geometry**
  - **W** = Gate Width
  - **L** = Gate Length
  - **t_{ox}** = thickness of gate oxide
  - **W/L** – defines transistor size
  - **L_{min}** = min. feature size

- **Semiconductor Construction**
  - **N-type** – mobile charge carriers are electrons (<u>n</u>egative charge)
  - **P-type** – mobile charge carriers are holes (<u>p</u>ositive charge)
  - **Doping** – add impurities to pure silicon to make material N-type or P-type
    - N_a – density of acceptor atoms - holes
    - N_d – density of donor atoms - electrons
  - **NMOS or N-channel** - electrons
    - Conductive channel is N-type
  - **PMOS or P-channel** - holes
    - Conductive channel is P-type
  - **Source & Drain** – doping implants into substrate to create n^+ & p^+ regions
  - **Oxide Layer** - Gate is isolated from substrate, which makes it high impedance, except for leakage

Construction of NMOS FET

Modified Graphic Courtesy of Kaushik Roy, Purdue
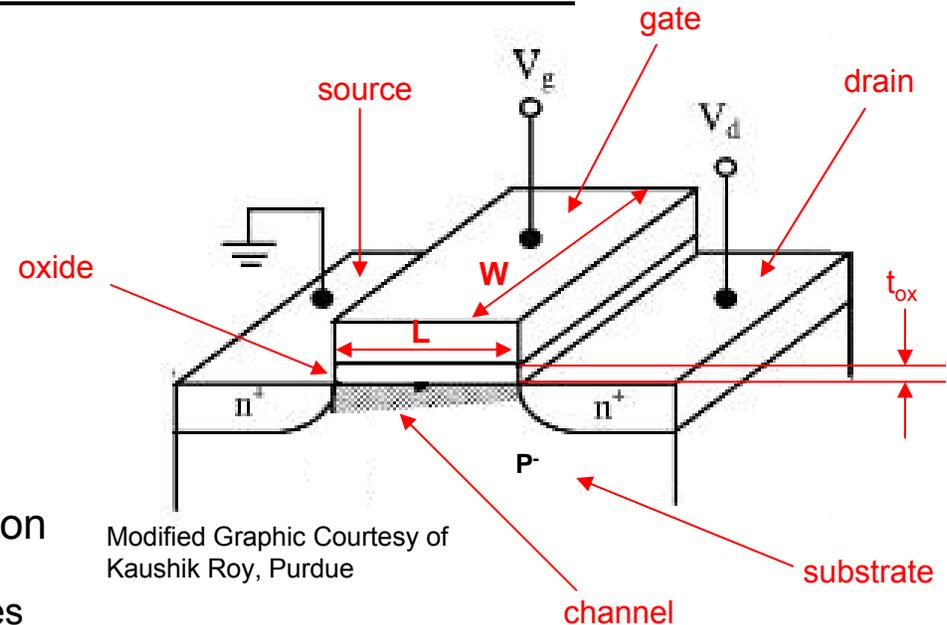
- **Operation**
  - Gate-Source voltage V_{GS} creates conduction channel under gate, allowing current to flow between drain & source
  - Minimum gate voltage to create channel called the Threshold Voltage V_{TH}

Survey of Feature Sizes
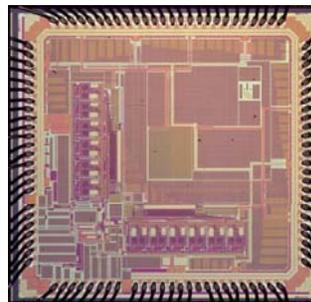## or
Size _DOES_ Matter!

Big is Good!

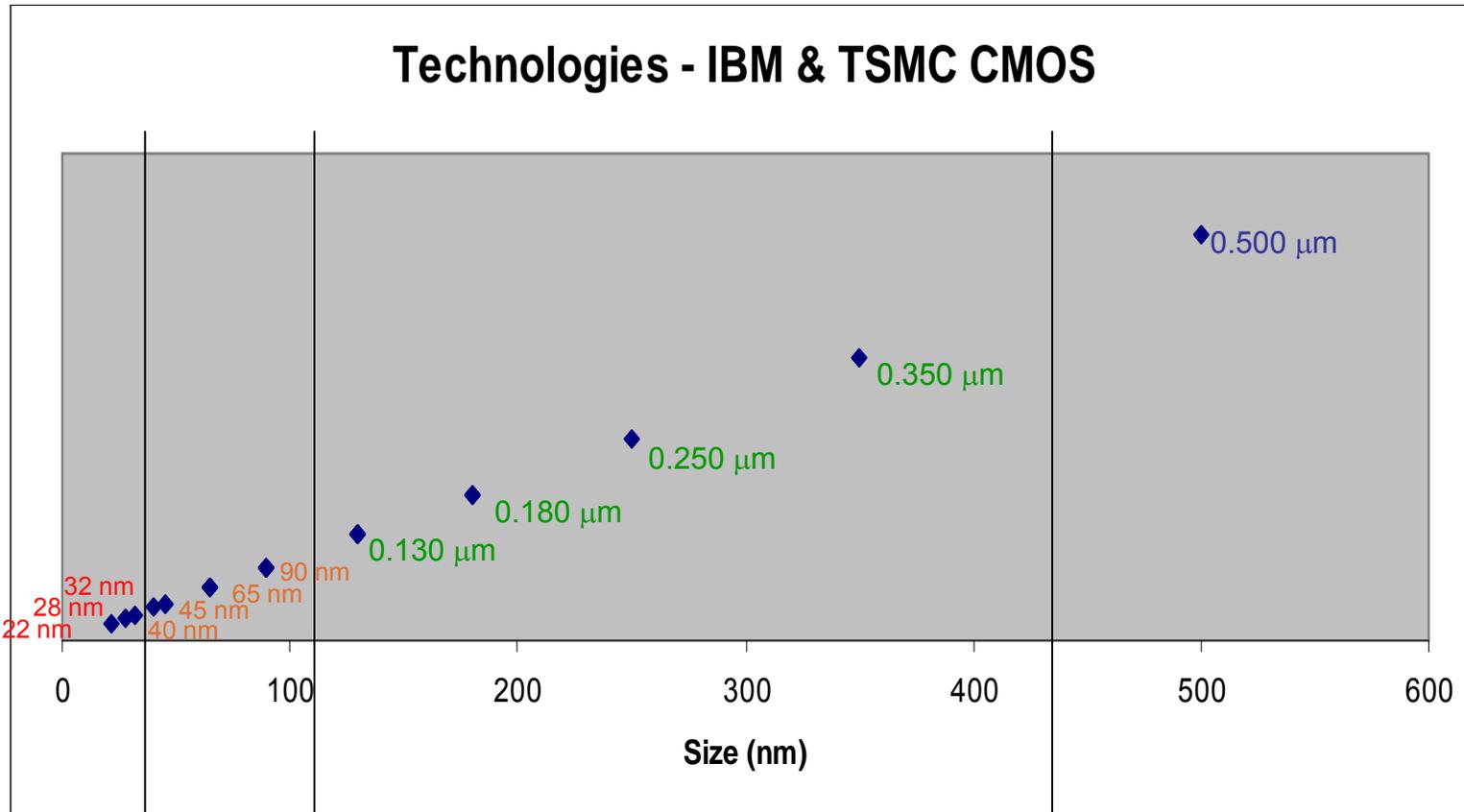*Big is Good?*

Big is Good!

Big is Good!

Small is Good.
But not too small…

Big is Good?

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Survey of Feature Sizes
IBM & TSMC CMOS Processes
Offered Through MOSIS Today

Technologies - IBM & TSMC CMOS

| Fab House	Feature Size	Process
IBM	22 nm	
IBM	28 nm	
IBM	32 nm	32SOI
TSMC	40 nm	CLN40/CMN40
IBM	45 nm	12SOI
TSMC	45 nm	CLN45/CMN45
IBM	65 nm	10SF
IBM	65 nm	10LPe/RFe
TSMC	65 nm	CLN65/CMN65
TSMC	65 nm	CMN65T
IBM	90 nm	9SF
IBM	90 nm	9LP/RF
TSMC	90 nm	CLN90/CMN90
TSMC	90 nm	CMN65T
IBM	0.130 μm	8RF-LM
IBM	0.130 μm	8RF-DM
TSMC	0.130 μm	CL013/CM013
TSMC	0.130 μm	CL013LP
TSMC	0.130 μm	CL013LV
IBM	0.180 μm	7SF
IBM	0.180 μm	7RF
IBM	0.180 μm	7RFSOI
IBM	0.180 μm	7HV
IBM	0.250 μm	6RF
IBM	0.350 μm	
IBM	0.500 μm	

Data from MOSIS

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The Basic Question:
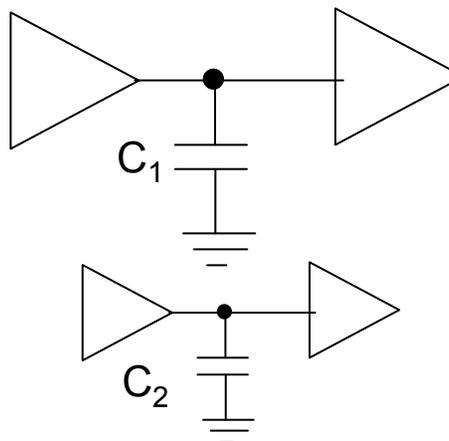## How to Achieve Faster (Higher BW) ASICS?

- ## The Basic Answer:

  - General trend:
    The smaller the feature size, the faster the chip can operate.

  - Why? A few high-level reasons:
    - ♦ Smaller size = <u>shorter distance</u> that signals need to propagate
    - ♦ Smaller size = generally <u>lower parasitic capacitance</u>
      (But watch out for larger capacitance/unit area…)
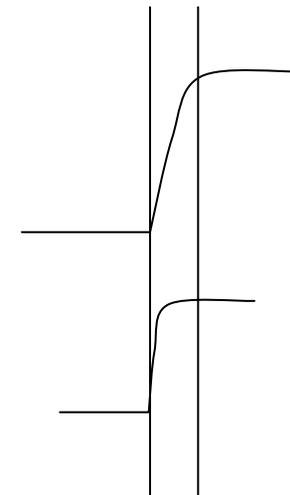   - ♦ Smaller size → <u>use lower voltage rails</u> → reach logic levels faster

    ⇨ ***More technical answers later…***
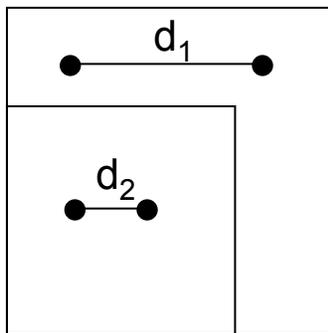
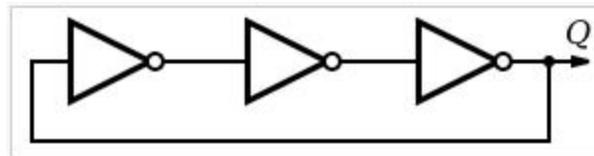**Shorter transmission distance**   **Smaller capacitances**   **Lower voltage rails**
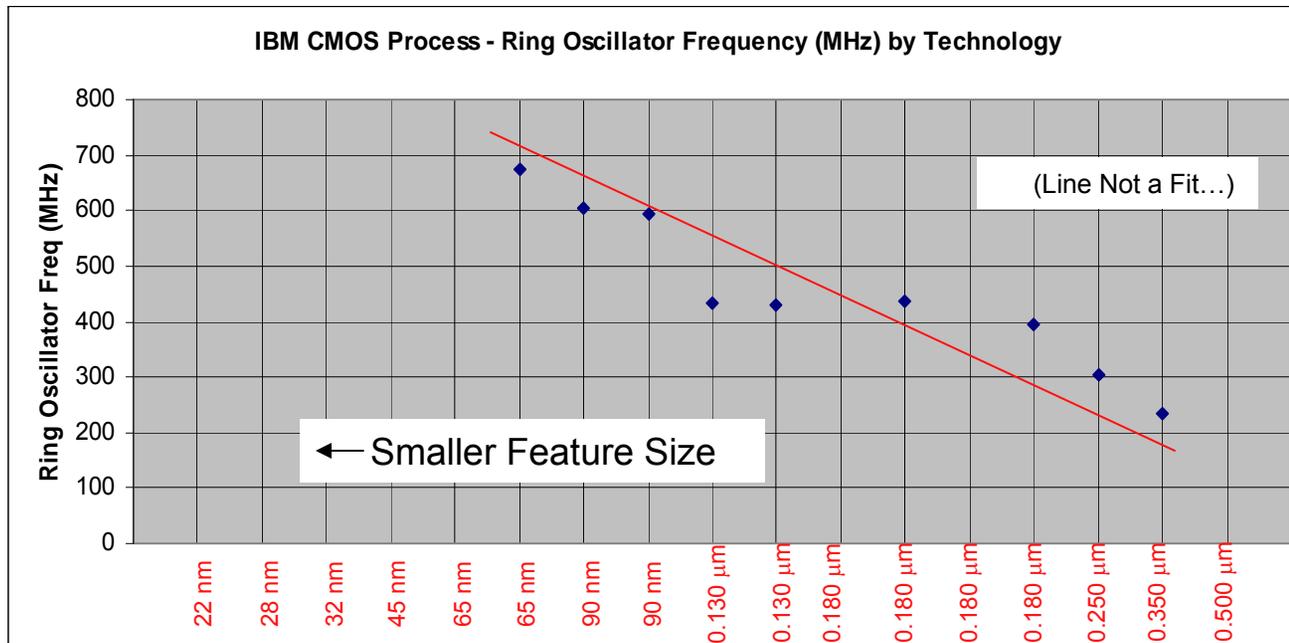
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The Basic Question:
How to Achieve Faster (Higher BW) ASICS? (Cont.)

- **Measurements Tell the Tale:**
  - One measure of speed in CMOS: Ring Oscillator Frequency
    - ♦ Basic test structure used by MOSIS to measure fabrication run acceptance
    - ♦ Generally configured as an odd number of inverters, minimum-sized devices
      $F_0 = 1/(2N * Inverter\_delay)$, N = # Inverters (MOSIS uses 31 stages.)

Courtesy Wikipedia

IBM CMOS Process - Ring Oscillator Frequency (MHz) by Technology

(Line Not a Fit…)

← Smaller Feature Size

Ring Oscillator Freq (MHz)

Feature Size	Process
22 nm	
28 nm	
32 nm	32SOI
45 nm	12SOI
65 nm	10SF
	10LPe/RFe
90 nm	9SF
	9LP/RF
0.130 μm	8RF-LM
	8RF-DM
0.180 μm	7SF
	7RF
	7RFSOI
	7HV
0.250 μm	6RF
0.350 μm	
0.500 μm	

Data from MOSIS

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How Feature Size Affects Speed

- **Robert Dennard's Scaling Law (1974)**
  - If scale the physical parameters of an integrated circuit equally by factor K, then performance parameters scale as follows:

Geometry & Supply voltage	L_g, W_g T_{ox}, V_{dd}	K	**Scaling K : K=0.7 for example**
Drive current in saturation	I_d	K	$I_d = v_{sat} W_g C_o (V_g - V_{th})$ C_o: gate C per unit area $\rightarrow W_g (t_{ox}^{-1})(V_g - V_{th}) = W_g t_{ox}^{-1}(V_g - V_{th}) = KK^{-1}K = K$
I_d per unit W_g	$I_d/\mu m$	1	I_d per unit $W_g = I_d / W_g = 1$
Gate capacitance	C_g	K	$C_g = \varepsilon_o \varepsilon_{ox} L_g W_g / t_{ox}$ $\rightarrow$ $KK/K = K$
Switching speed	τ	K	$\tau = C_g V_{dd}/I_d$ $\rightarrow$ $KK/K = K$
Clock frequency	f	1/K	$f = 1/\tau = 1/K$
Chip area	A_{chip}	α	α: Scaling factor $\rightarrow$ **In the past, $\alpha > 1$ for most cases**
Integration (# of Tr)	N	α/K^2	$N \rightarrow \alpha/K^2$ $= 1/K^2$, when $\alpha = 1$
Power per chip	P	α	$fNCV^2/2 \rightarrow K^{-1}(\alpha K^{-2})K(K^1)^2 = \alpha$ $= 1$, when $\alpha = 1$

| Device or Circuit Parameter	Scaling Factor
Device dimension t_{ox}, L, W	K
Doping concentration N_a	1/K
Voltage V	K
Current I	K
Capacitance eA/t	K
Delay time per circuit VC/I	K
Power dissipation per circuit VI	K^2
Power density VI/A	1

Table Courtesy of Mark Bohr, IBM

Slide Courtesy of Hiiroshi Iwai, Tokyo Institute of Technology

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How Feature Size Affects Speed (Cont.)

- **Dennard's Scaling Law & Moore's Law**
  - **Gordon Moore's Law:** "The number of transistors that can placed inexpensively on an integrated circuit doubles approximately every two years." → Basis for Industry Roadmap (ITRS)
  - **Dennard:** If scale physical dimensions by K, then area of chip ~ K^2
    - ♦ For K ~0.7 ~ 1/SQRT(2), $K^2 \sim \frac{1}{2}$ → X2 more transistors for a given die size
  - **Industry:** Ratios between successive technology steps: 350/500 = 0.7; 250/350 = 0.71; 90/130 = 0.69; 65/90 = 0.722

Plots Courtesy of Mark Bohr, IBM
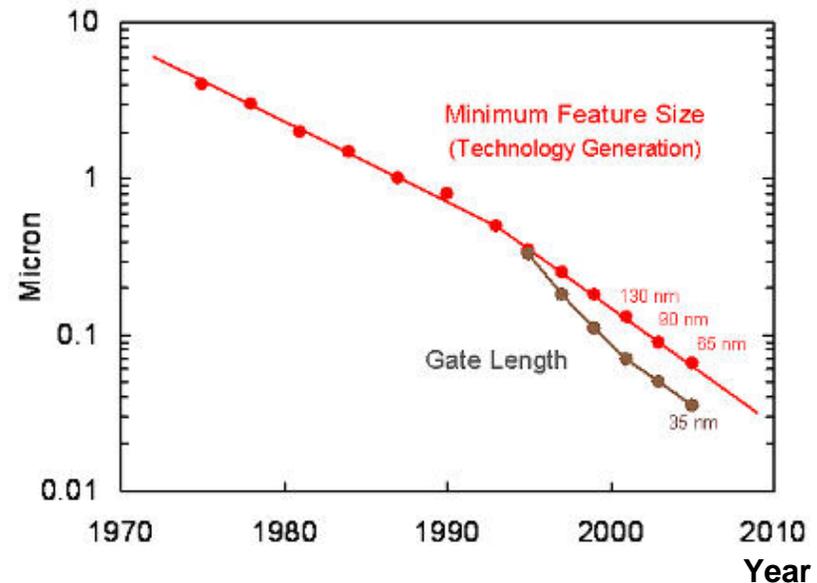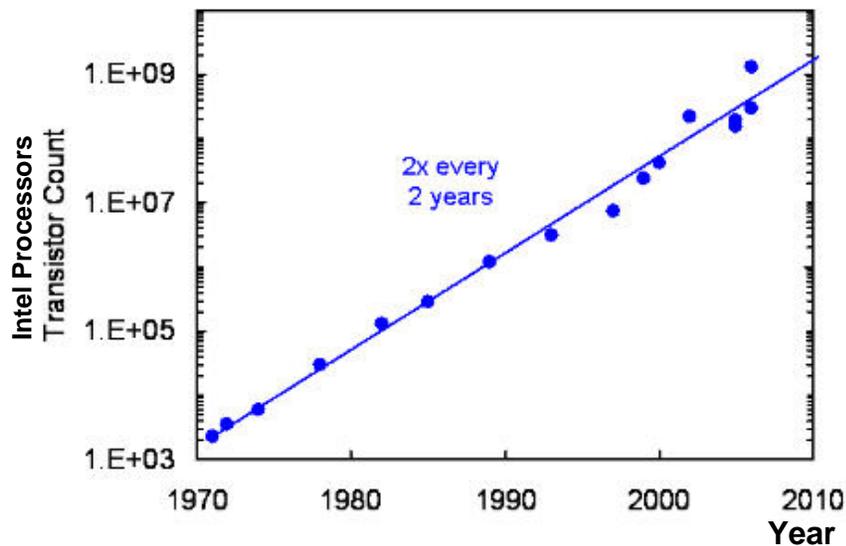
Moore's Law will come to an end in ~2014, when the feature size approaches a few atomic layers.
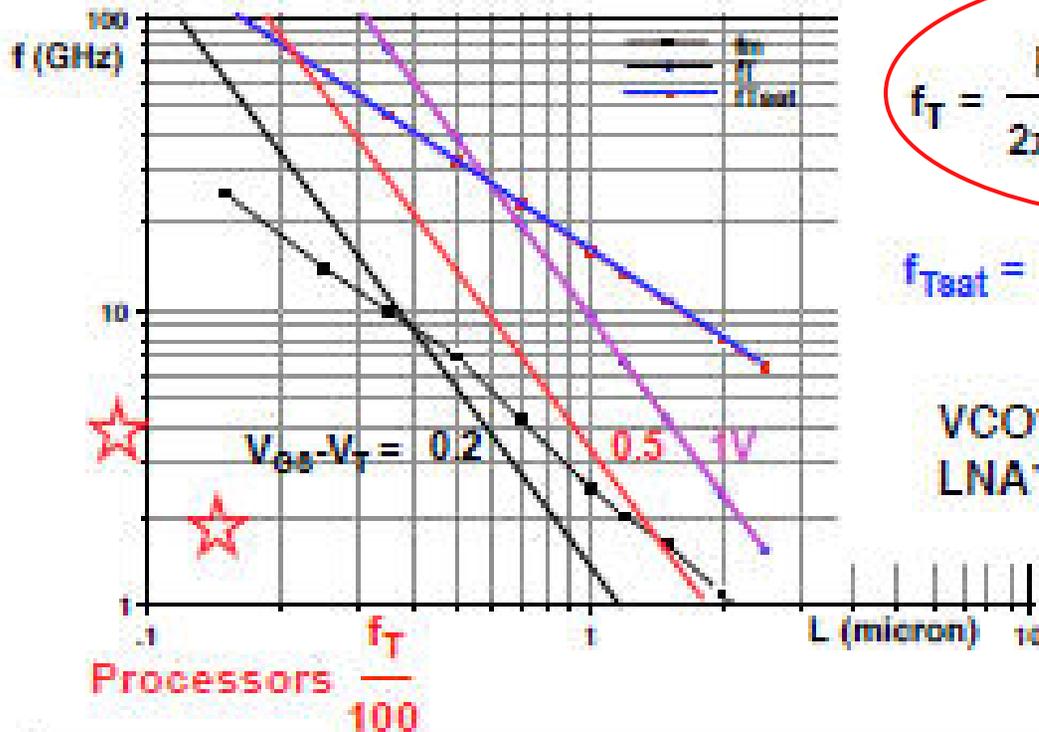
How Feature Size Affects Speed (Cont.)

- **Examining Speed versus Technology**
  - A technical answer from semiconductor physics (Courtesy of Willy Sansen):

Maximum f_T versus channel length L   **(f_T = Freq. where current gain = 1)**

$$f_T = \frac{\mu}{2\pi L^2} \underbrace{(V_{GS}-V_T)}_{0.2 \dots 1\,V}$$

$$f_{Tsat} = \frac{v_{sat}}{2\pi L}$$

VCO's
LNA's $\dfrac{f_T}{5}$

Critical Parameters:
- Mobility
- Channel Length
- Thresh. Voltage
- $V_{GS}-V_T$

⇨ *These are functions of the technology…*

Processors $\dfrac{f_T}{100}$

Willy Sansen   New Delhi 1-02 15

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How Feature Size Affects Speed (Cont.)

- **Examining Speed versus Technology (Cont.)**
  - Unity Gain Frequency:

$$f_T = \frac{\mu}{2\pi L^2}(V_{GS} - V_T)$$

Critical Parameters:
- Mobility
- Channel Length
- Thresh. Voltage
- V_{GS}-V_T

  - Length L

    ⇨ *Decreases as feature size decreases, L α K scaling, for K < 1*
      ⇨ *Causes f_T to increase as $1/K^2$ for K < 1*

  - Carrier Mobility

$$\mu = \mu_o + \frac{\mu_1}{1 + (\frac{N}{N_{ref}})^\alpha}$$ ➡ $$\mu_n(N_D) = 65 + \frac{1265}{1 + (\frac{N_D}{8.5\times10^{16}})^{0.72}}$$
$$\mu_p(N_A) = 48 + \frac{447}{1 + (\frac{N_A}{6.3\times10^{16}})^{0.76}}$$

⇨ *N_D α 1/K → Increases for K<1*
  ⇨ *f_T decreases for K<1, but slowly…*

  - V_T & $(V_{GS} - V_T)$?
    - Want $(V_{GS} - V_T)$ as large as possible
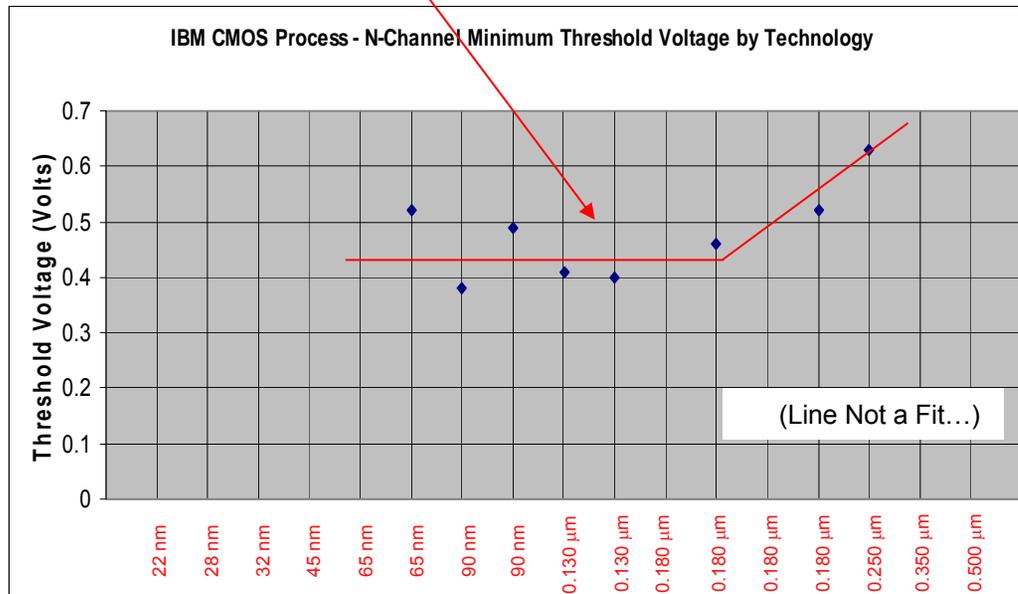   - Want V_T as small as possible

How Feature Size Affects Speed (Cont.)

- **Examining Speed versus Technology (Cont.)**

  - Generally, threshold voltage V_{TH} gets smaller with feature size
    - ◆ Partly a consequence of decreasing V_{dd}
    - ◆ Partly a consequence of increasing C_{OX} (aF/μm^2 gate area)
  - But, are approaching a limit with submicron technologies… Why?

$$V_{th} = V_{fb} + 2\psi_B + \frac{\sqrt{2\varepsilon_{si}qN_a\left(2\psi_B + V_{bs}\right)}}{C_{ox}}$$

where V_{fb} is the flatband voltage,
v_T = kT/q
C_{OX} is the gate oxide capacitance/area
ψ_B is the zero bias mobility
V_{bs} is the max. depletion layer width
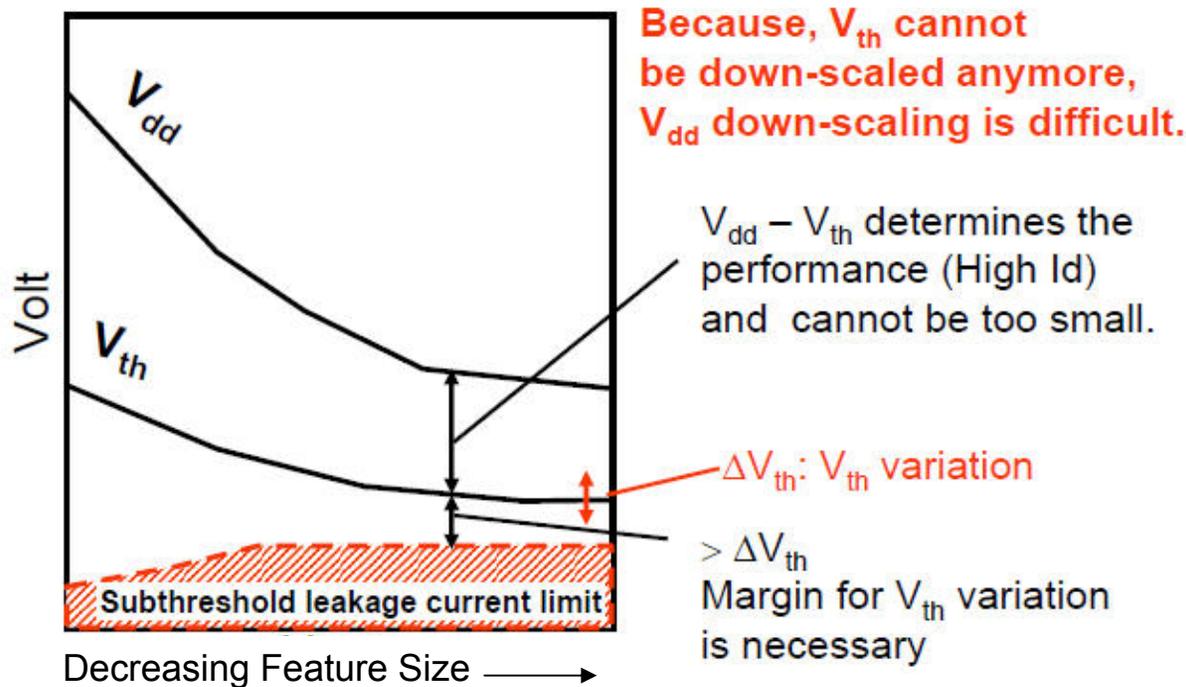N_a is the acceptor doping density

IBM CMOS Process - N-Channel Minimum Threshold Voltage by Technology

Threshold Voltage (Volts): 0, 0.1, 0.2, 0.3, 0.4, 0.5, 0.6, 0.7

(Line Not a Fit…)

Feature sizes (x-axis): 22 nm, 28 nm, 32 nm, 45 nm, 65 nm, 65 nm, 90 nm, 90 nm, 0.130 μm, 0.130 μm, 0.180 μm, 0.180 μm, 0.180 μm, 0.180 μm, 0.250 μm, 0.350 μm, 0.500 μm

Feature Size	Process
22 nm	
28 nm	
32 nm	32SOI
45 nm	12SOI
65 nm	10SF
	10LPe/RFe
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0.180 μm	7SF
	7RF
	7RFSOI
	7HV
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0.350 μm	
0.500 μm	

Data from MOSIS

How Feature Size Affects Speed (Cont.)

- **Examining Speed versus Technology (Cont.)**
  - V_{dd} scales with K, so V_{dd} decreases with smaller feature size
    - ♦ Difficulty in Down-scaling of Supply Voltage: Vdd

Because, V_{th} cannot be down-scaled anymore, V_{dd} down-scaling is difficult.

$V_{dd} - V_{th}$ determines the performance (High Id) and cannot be too small.

ΔV_{th}: V_{th} variation

$> \Delta V_{th}$ Margin for V_{th} variation is necessary

Volt

Vdd

Vth

Subthreshold leakage current limit

Decreasing Feature Size ⟶

How Feature Size Affects Speed (Cont.)

- **Examining Speed versus Technology (Cont.)**
  - Bottom Line - Unity Gain Frequency of FETs:

Decreases as $(K)^{0.7}$

$$f_T = \frac{\mu}{2\pi L^2} (V_{GS} - V_T)$$

Approaching a constant

Scales with K

⇨ **So, $f_T \propto 1/K$ (approximate)**

⇨ **i.e., f_T increases as feature size decreases**

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Consequences of Deep Submicron Technologies

- **Scaling Laws worked well until ~ 100 nm and smaller**
  - Performance generally well-predicted > 100 nm
  - Below 100 nm, start to see second-order and higher-order effects that affect performance
    - ♦ Especially for analog IC or mixed-signal ICs

- **Direct Performance Effects**
  - ***Increased leakage currents***
    - ♦ Increased power consumption
  - Transistor size mismatch
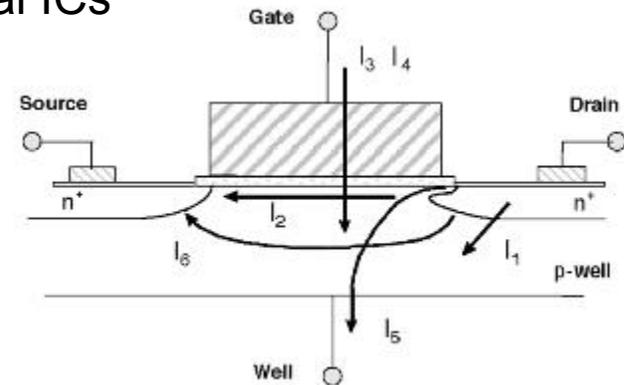
- **Other Performance Factors → Especially for Analog**
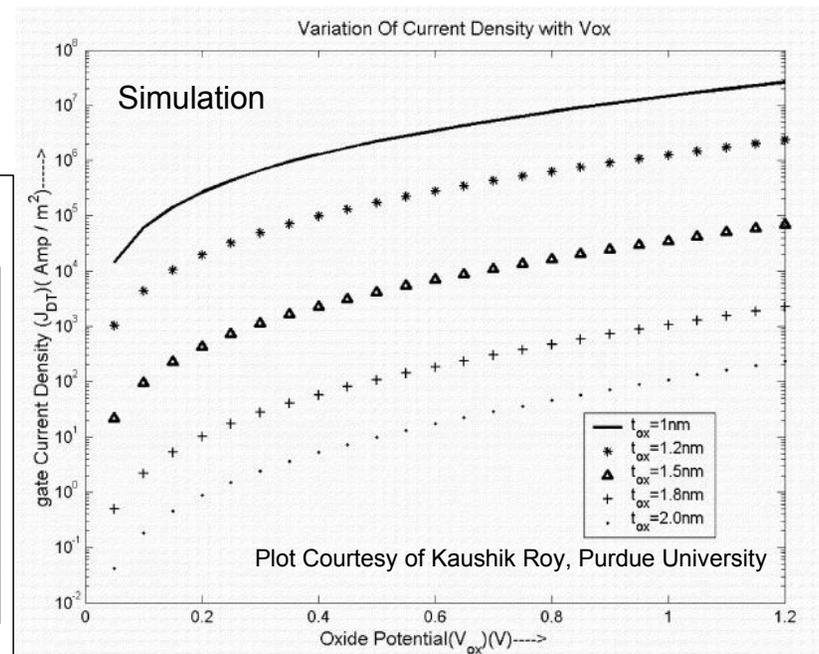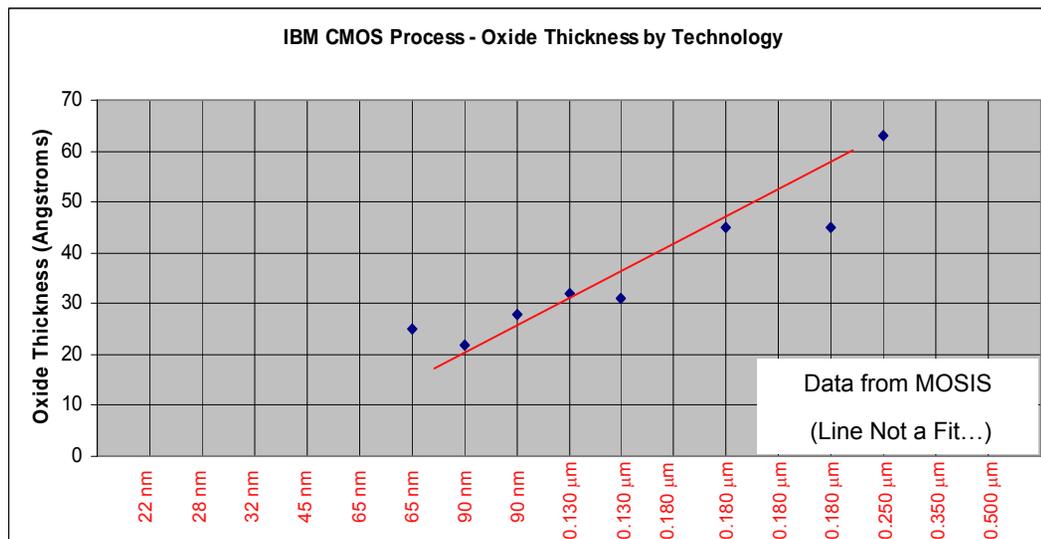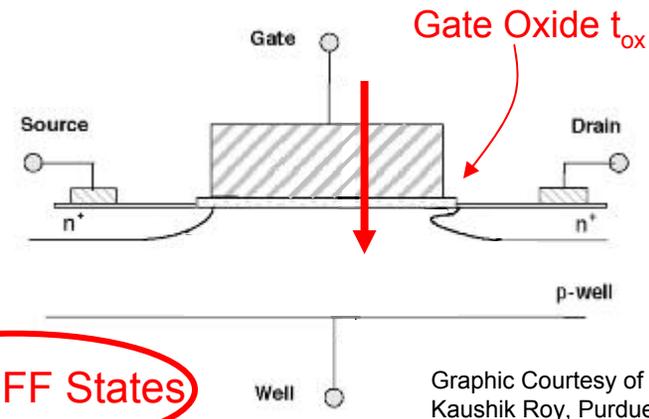 - Reduced voltage rails
  - Decreased signal-to-noise
  - Decreased dynamic range
  - Increased power density

Graphic Courtesy of
Kaushik Roy,
Purdue University

Consequences of Deep Submicron Technologies
(Continued)

- **Leakage Currents**
  - Gate oxide tunneling leakage (I_G)
    - ♦ Thin gate oxides allow electron tunneling from gate to substrate
    - ♦ **Major source of leakage current in sub-micron CMOS**
    - ♦ The thinner the oxide, the worse the leakage current, i.e. the smaller the feature size, the worse the leakage current, since t_{ox} scales

Gate Oxide t_{ox}

ON & OFF States

Graphic Courtesy of Kaushik Roy, Purdue

IBM CMOS Process - Oxide Thickness by Technology

Data from MOSIS
(Line Not a Fit...)

Variation Of Current Density with Vox

Simulation

Plot Courtesy of Kaushik Roy, Purdue University

Consequences of Deep Submicron Technologies
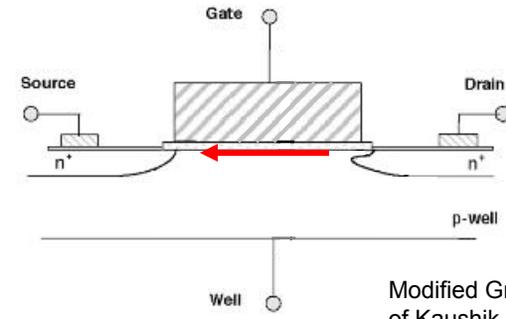## (Continued)

- **Leakage Currents (Cont.)**
  - Subthreshold leakage (I_{SUB})
    - ♦ Drain-source current during weak inversion, $V_{GS} < V_{TH}$
    - ♦ Dominated by diffusion current of minority carriers, rather than drift current that dominates in strong inversion
    - ♦ Carriers move along surface
    - ♦ Very sensitive to process parameters, device size, supply voltage, and temperature

$$I_{ds} = \mu_0 C_{ox} \frac{W}{L} (m-1)(v_T)^2 \times e^{(V_g - V_{th})/mv_T}$$
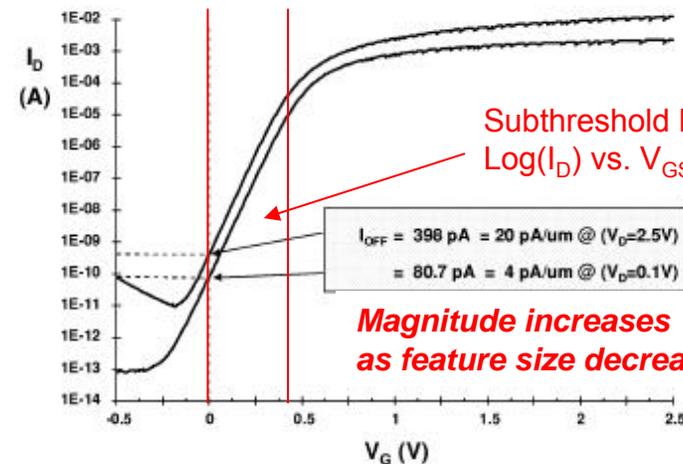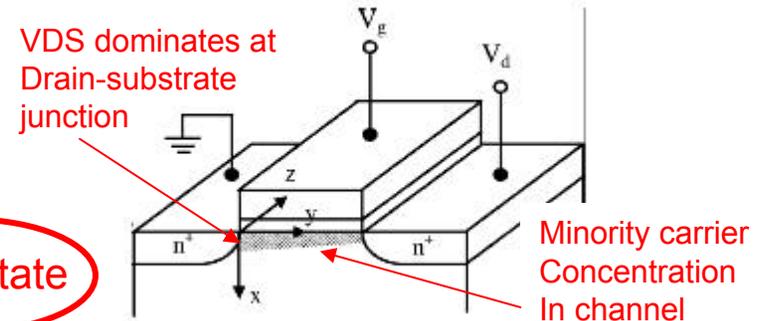$$\times \left(1 - e^{-v_{DS}/v_T}\right)$$

where

$$m = 1 + \frac{C_{dm}}{C_{ox}} = 1 + \frac{\frac{\varepsilon_{si}}{W_{dm}}}{\frac{\varepsilon_{ox}}{t_{ox}}} = 1 + \frac{3t_{ox}}{W_{dm}}$$

where V_{th} is the threshold voltage,
$v_T = kT/q$
C_{OX} is the gate oxide capacitance
μ_{OX} is the zero bias mobility
W_{dm} is the max. depletion layer width

Modified Graphic Courtesy of Kaushik Roy, Purdue

VDS dominates at Drain-substrate junction

OFF State

Minority carrier Concentration In channel

Subthreshold Leakage Log(I_D) vs. V_{GS}

$I_{OFF} = 398$ pA $= 20$ pA/um @ ($V_D = 2.5$V)
$= 80.7$ pA $= 4$ pA/um @ ($V_D = 0.1$V)

Magnitude increases as feature size decreases

Graphics Courtesy of Kaushik Roy, Purdue University

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Consequences of Deep Submicron Technologies
(Continued)

- **Leakage Currents (Cont.)**
  - PN Junction Reverse-Bias Leakage (I_{REV})
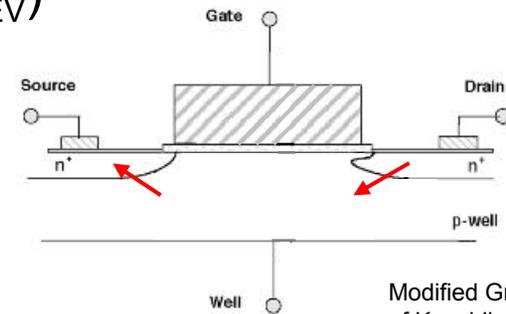   - ♦ 2 mechanisms
   - Minority-carrier drift/diffusion
      - Electron-hole generation
    - ♦ Occurs when P & N junctions are heavily doped
      - Doping (N_a & N_d) increases as feature size decreases → Leakage increases as feature size decreases
      - Causes band-to-band tunneling (BTBT) due to electric field from the doping

$$E = \sqrt{\frac{2qN_aN_d(V_{app} + V_{bi})}{\varepsilon_{si}(N_a + N_d)}}$$
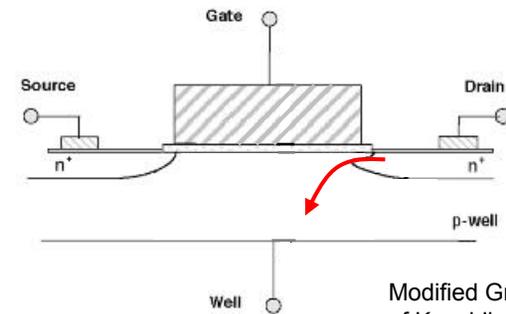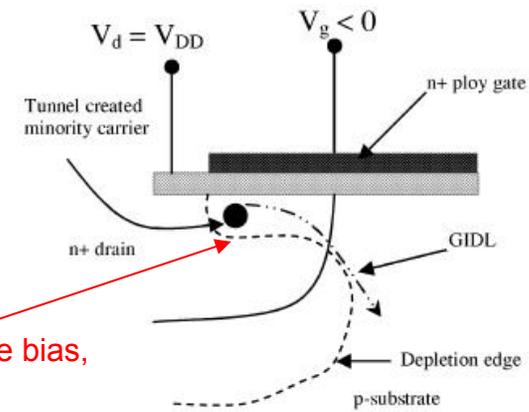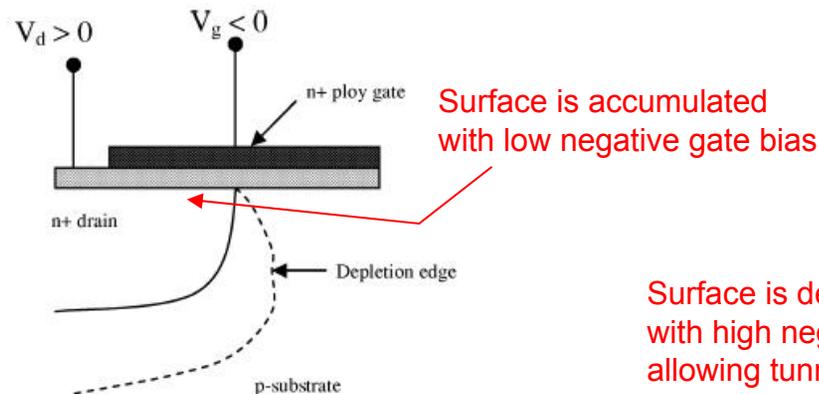
Modified Graphic Courtesy of Kaushik Roy, Purdue

ON & OFF States

Graphics Courtesy of Kaushik Roy, Purdue University
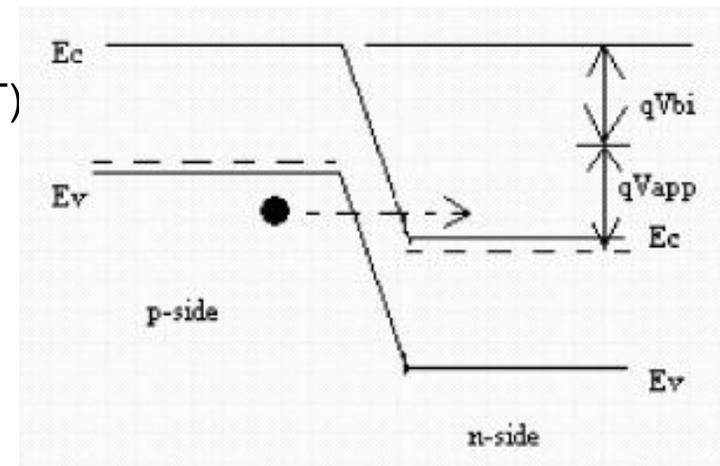
Consequences of Deep Submicron Technologies
(Continued)

- **Leakage Currents (Cont.)**
  - Gate Induced Drain Leakage (I_{GIDL})
    - ◆ Caused by narrowing of depletion region around drain when FET is off
      - – Due to electric field between gate and drain
    - ◆ Get tunneling of minority carriers from drain to substrate
    - ◆ Strong function of
      - – Doping profile at drain edge
      - – Oxide thickness
      - – V_{dd}

Modified Graphic Courtesy of Kaushik Roy, Purdue

OFF State

Graphics Courtesy of Kaushik Roy, Purdue University

Surface is accumulated with low negative gate bias

Surface is depleted with high negative gate bias, allowing tunneling of minority carriers into substrate
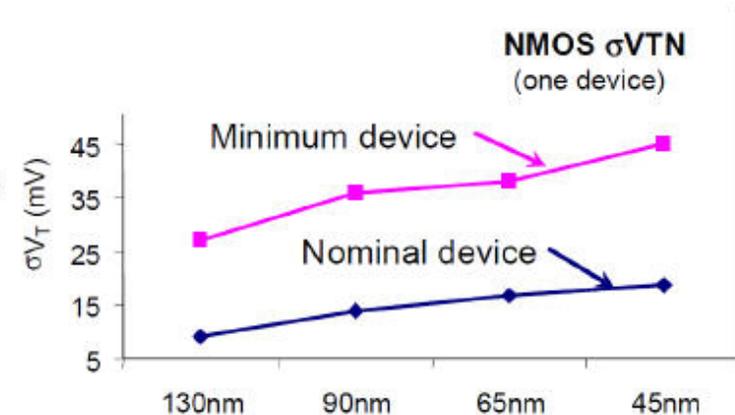
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Consequences of Deep Submicron Technologies
(Continued)

- ## **Matching Problems**

  - Generally, device matching becomes worse as feature size decreases

    - ♦ Limitations of lithography & processing

Threshold voltage mismatch A_{VT}

$A_{VT} \sim t_{ox} \sqrt[4]{N_B}$

1 mVμm /nm t_{ox}

Willy Sansen New Delhi 1-09 21

Plot Courtesy of
Willy Sansen

NMOS σVTN
(one device)

Minimum device

Nominal device
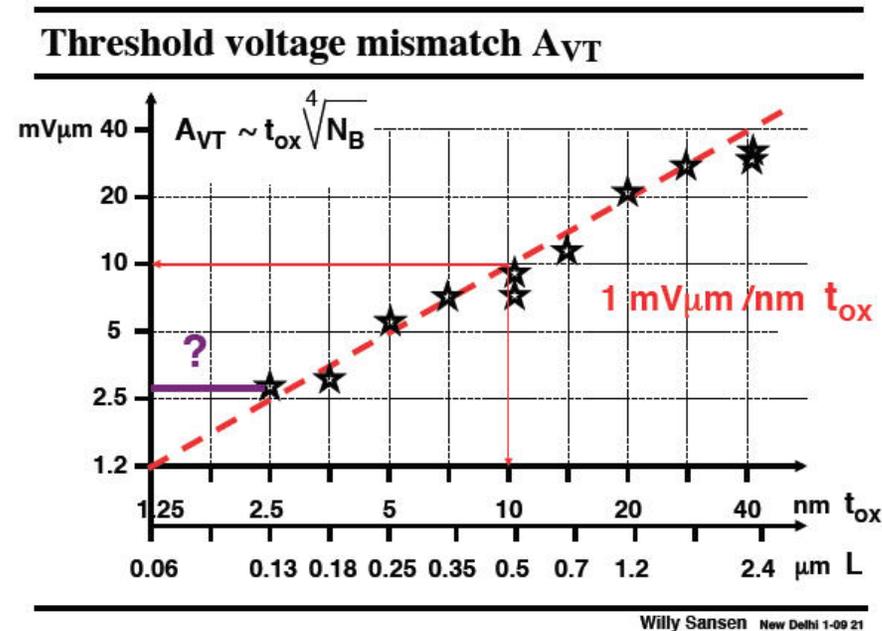
Plot Courtesy of
Hiroshi Iwai,
Tokyo Institute of Technology

⇨ *Slope is gentle …*
⇨ *Many designs may not be affected …*

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Other Consequences of Deep Submicron Technologies

- **Reduced Headroom**
  - Circuits with more than ~2-3 transistors between V_{dd} and V_{ss} run out of head room due to reduced V_{dd} (scales with K…)

- **Reduced Signal-to-Noise**
  - Reduced voltage rails mean smaller signals
  - Noise may not improve with smaller feature size
    - ♦ Depends on design…

- **Reduced Dynamic Range**
  - Also a consequence of reduced voltage rails and higher noise…

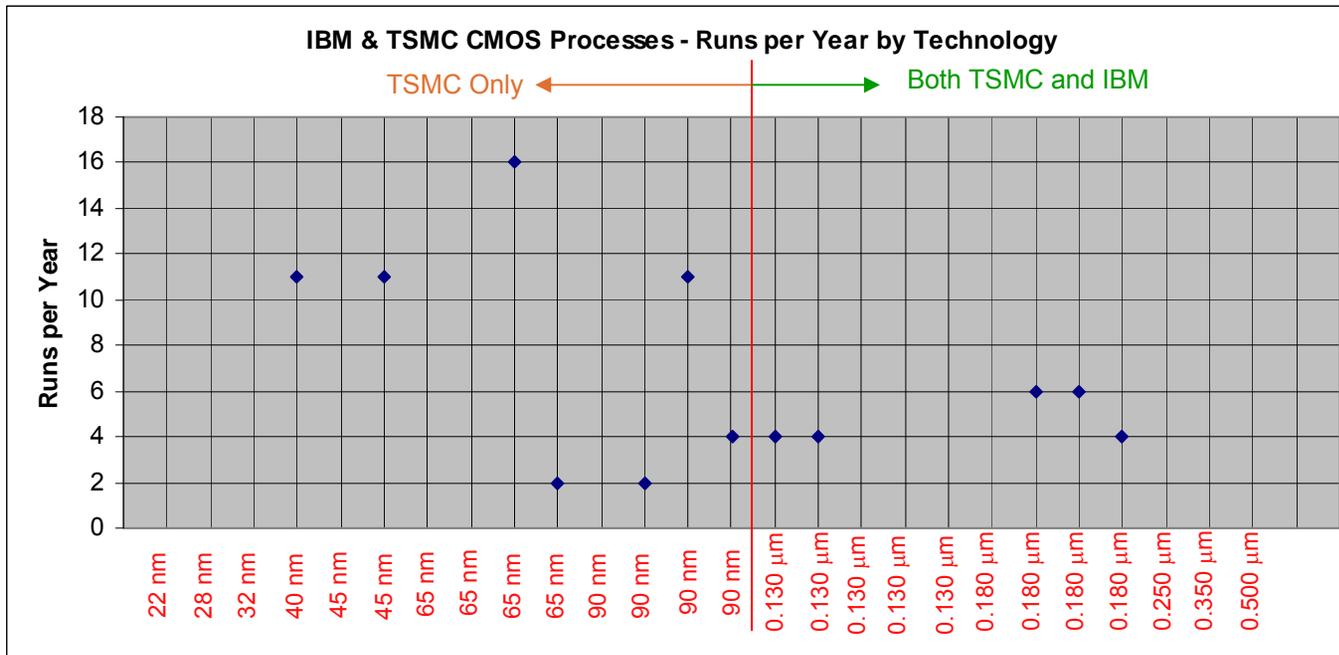- **Increased Power Density**
  - Consequence of leakage currents

⇨ *For digital, these are mostly OK*
⇨ *For analog, can be a problem…*

Practical Considerations

- ## Availability (through MOSIS)

  - Currently, technologies between 40-100 nm only offered by TSMC
    - ♦ Even then, models sparse or not available
  - IBM: Only trusted vendors below 130 nm

IBM & TSMC CMOS Processes - Runs per Year by Technology

TSMC Only ← → Both TSMC and IBM

Fab House	Feature Size	Process
IBM	22 nm	
IBM	28 nm	
IBM	32 nm	32SOI
TSMC	40 nm	CLN40/CMN40
IBM	45 nm	12SOI
TSMC	45 nm	CLN45/CMN45
IBM	65 nm	10SF
IBM	65 nm	10LPe/RFe
TSMC	65 nm	CLN65/CMN65
TSMC	65 nm	CMN65T
IBM	90 nm	9SF
IBM	90 nm	9LP/RF
TSMC	90 nm	CLN90/CMN90
TSMC	90 nm	CMN65T
IBM	0.130 μm	8RF-LM
IBM	0.130 μm	8RF-DM
TSMC	0.130 μm	CL013/CM013
TSMC	0.130 μm	CL013LP
TSMC	0.130 μm	CL013LV
IBM	0.180 μm	7SF
IBM	0.180 μm	7RF
IBM	0.180 μm	7RFSOI
IBM	0.180 μm	7HV
IBM	0.250 μm	6RF
IBM	0.350 μm	
IBM	0.500 μm	

Practical Considerations

- **Cost**
  - (Costs unknown for every technology at press time…)
  - Generally, leading-edge technologies very expensive, even through MOSIS

- **Models**
  - Models are poor – to – non-existent for leading-edge technologies
  - Customer support is poor for leading-edge technologies
  - MOSIS data not available for leading-edge technologies

- **General Difficulty**
  - Expect long learning curve with the more advanced technologies

Summary

- **For high-speed and high-bandwidth, generally want technologies with smaller feature size**
  - Smaller distances
  - Smaller parasitic capacitances
  - Smaller voltage swings
  - Intrinsically faster devices (from scaling law principles)
- **Below ~ 100 nm, start to have higher-order problems**
  - Leakage currents of various kinds can affect designs
    - ♦ Higher internal power
    - ♦ May significantly affect analog circuits, in particular sample & hold circuits
  - Matching of transistors is worse
  - Signal headroom is reduced
  - Dynamic range is reduced
- **Prospects for near future**
  - Scaling laws have worked beautifully for 40 years, but we're reaching a hard limit
  - Industry has kept pace, but will have difficulty below 10 nm
  - Leading-edge technologies difficult to use right now, but this will improve
  - Not clear if higher-order process problems can be solved for analog use…
  - Perhaps clever circuit design can be employed, but this will take time…

⇨ *130 nm technology is not a bad place to be right now for analog work…*

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