Noise limitations in SCA.

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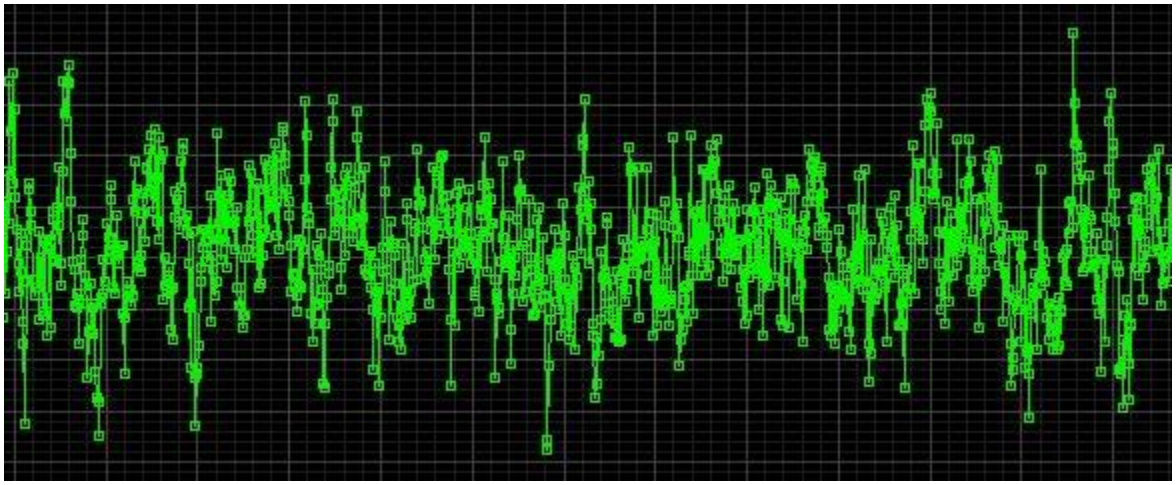


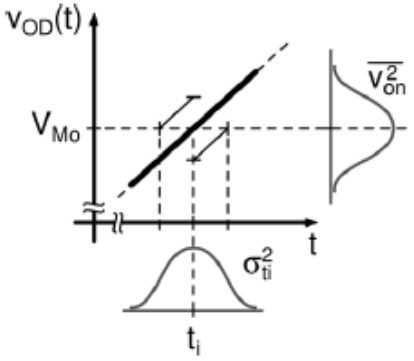
Relation between noise & jitter.

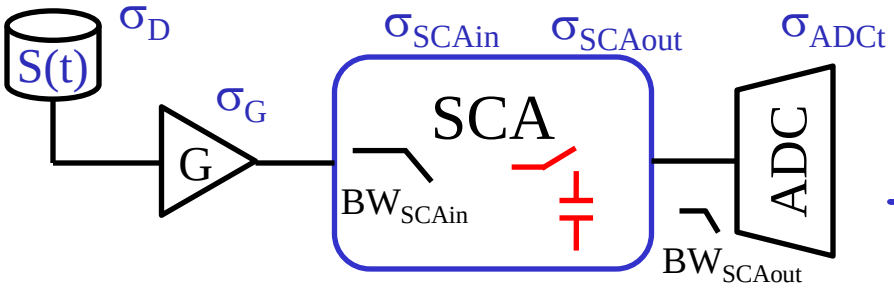
$\sigma_t = \sigma_V \ . \ dV/dt$

"Low" frequency noise can be rejected digitally

(baseline subtraction, digital filter, digital CFD…)

dV/dt is proportional to A/BW





$$\sigma_V^2 = G(\sigma_D^2 + 2\sigma_G^2) + \sigma_{SCAin}^2 + \sigma_{SCAout}^2 + \sigma_{ADC}^2$$

$$A(t) = G.\ S(t)$$

- σ_D and σ_G are the contribution of detector + amplifiers: scales as $BW^{1/2}$.
- σ_{SCA} contribution of the SCA
  - σ_{SCAin} part scales as $BW_{SCAin}^{1/2}$.
  - σ_{SCAout} after the sampling) is independent of BW_{SCAin}
- σ_{ADC} digitization noise (including quantization noise (LSB/ $12^{1/2}$).

« 2nd Stage »

Switches in scaled down technologies.

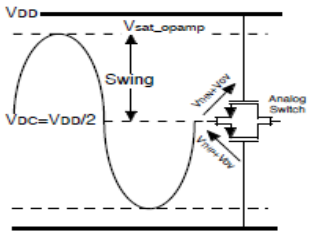
- MOS switch Ron resistance given by :

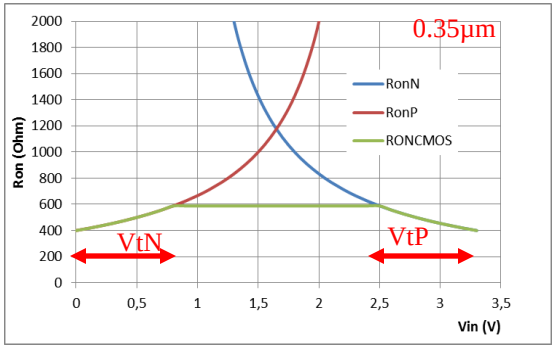
$$R_{ON} \approx \frac{1}{g_{ds}} = \frac{1}{\mu * C_{ox} \frac{W}{L}(V_{gs} - V_{th})}$$

Highly non linear

- Usually it is linearized by using NMOS & PMOS in parallel and swing set to ~VDD/2

© Baschirotto

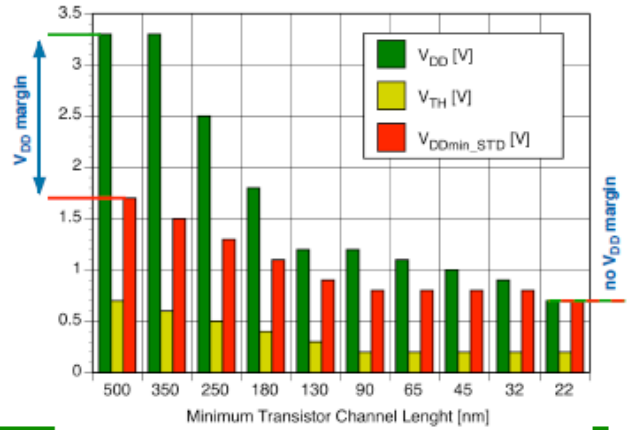


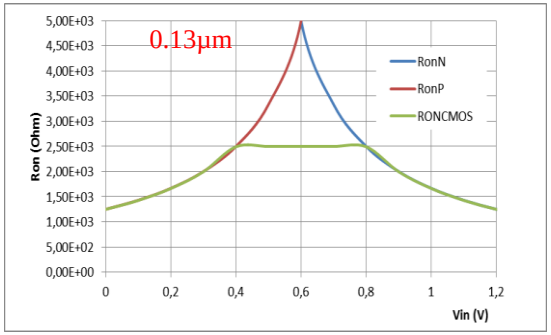


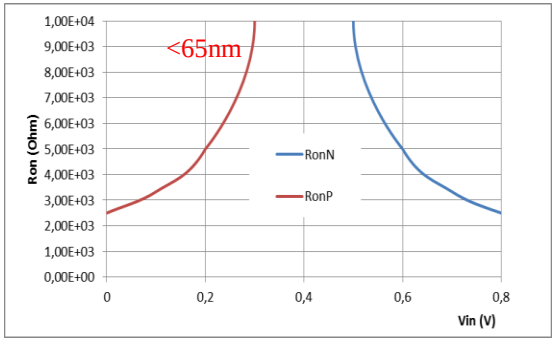
- In advanced technologies:

VDD is reduced , VTH also but not in the same ratio => max signal decrease.

CMOS switches linear region is smaller & smaller

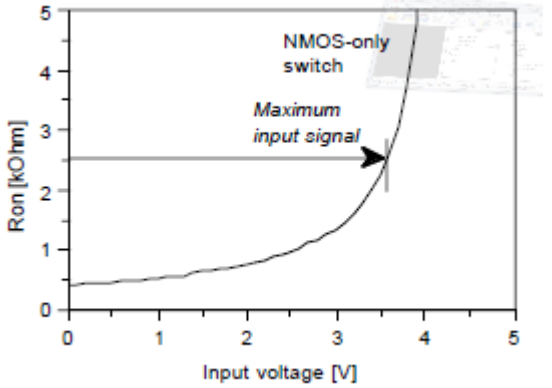




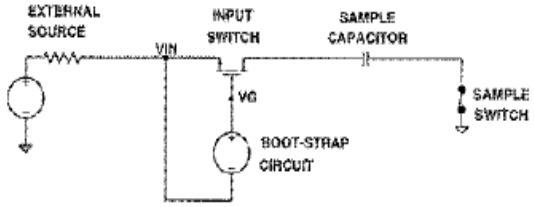


Max signal decreasing with technology scaling.

- In advanced technologies:
  - CMOS switch less useful => use of NMOS only switch. Swing now centered near gnd.
    => can be a good thing as PMOS switches (3 x larger than NMOS switches) are heavily loading the input SCA input (lumped RC on the input bus)
  - But R_{on} now vary a lot with Vin: => BW vary with Vin
    $\Rightarrow$ Distorsion => poor ENOB



  - Solutions (can be cumulative):
    - Limit the input swing to stay in the linear region.
    - On-chip clock mulitplication
    - Bootstraped switch (VGS-VT= cte) used in modern ADCs.
      Need for extra capa on the input bus. Feasible in a SCA ?

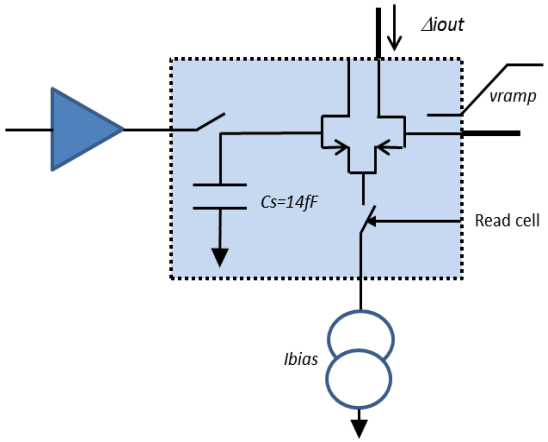


    - Differential input : swing multiplied by 2. Effect of non constant Ron averaged.

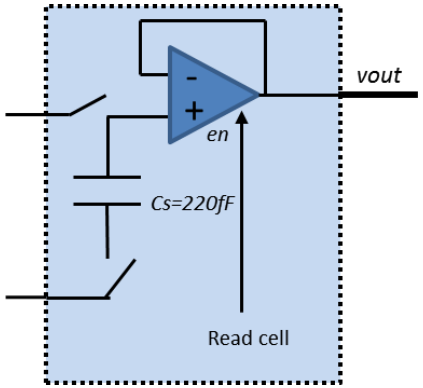
In any case A reduced => need some effort on σ_V to get a good time resolution.

Noise source in SCAs

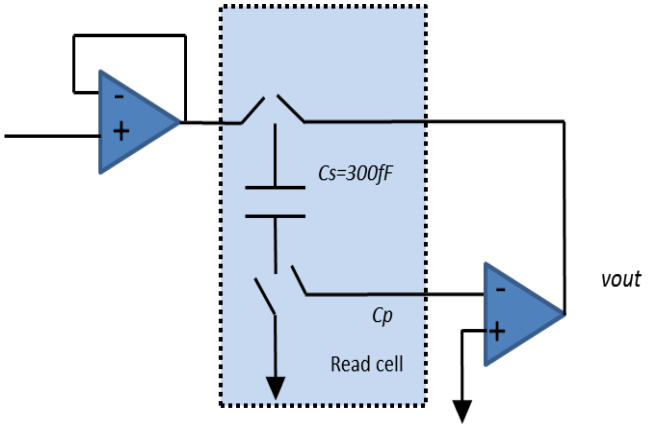
- Very architecture dependent . 3 family of designs studied:



A la Target:
Buffered SH
Wilkinson Readout
Very Small Cs



A la DRS:
Unbuffered diff SH
Closed Loop Follower readout.



A la SAM:
Buffered SH
Fed Back OPAMP readout
Fully differential

- But Common features/rules are existing.
  - 4 kinds of "noise" can be distinguished:
    - The noise due to artefacts.
    - The pickup noise / D->A coupling / Power supply noise
    - "Dynamic" noise : distorsion, non linearities…
    - The intrinsic electronic noise : the most easy to understand and to manage

Noise due to artefacts.

- Unwanted behavior of the digital part : metastablity …
- Ghost pulses : the old events are not fully erased before a new is written in the SCA
  => memory of a previous pulse.
  ⇒ Dielectric absorption problems reported in the SCA of early 90s.

- XTALK in some special cases (mixing of signal with very different amplitudes, saturation).

- Coupling between input and output
  ⇒ All the high impedance nodes of the SCA are perfect receivers (capacitive coupling) for the high frequency input signals.
  ⇒ The output impedance of a closed loop OTA is high at high frequency.

- In the following slides we assume that some "fix pattern" spread (offset, gain) can be corrected offline
  ⇒ valid only if stable (with time, temperature…):
  ⇒ Mor stable if closed loop or differential structures
  ⇒ If not, they are randomized and are contributing to noise.

Noise due to couplings : may affect operation during sampling or readout

- On and off chip D->A coupling:

  - Very dependent on layout, technology and substrates.
  - In SCAs, we are obviously in very favorable situation :
    - No gain in intrinsic part of the SCAs (excepted the hidden ones).
    - Any idea of what happens when x10 or 20 gain integrated in the chip ?

  - Minimize high impedance nodes.
  - Larger Cs => Larger robustness
  - The couplings which are synchronous with the sampling clock (or dividers) are often reproducible and may be seen as “pedestals”.
  - Avoid asynchronous clocks or asynchronous signal dispatched everywhere.
  - Differential signaling helps a lot (If CMR still exists @ HF)

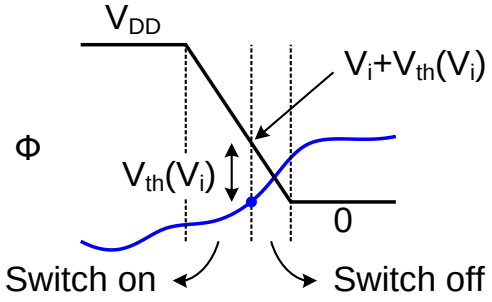
Noise from power supplies

- External noise (ie from DC-DC converters).
- Noise can be generated by outside digital logic or by the activity of the chip itself

- Sensitivity to the power supplies (PSRR):
  - Closed loop structure are more robust (esp. if using OPA) , but very scales as open loop gain.
  - Differential operation helps a lot.
  - Worst when VDD is smaller.

Dynamic « noise »

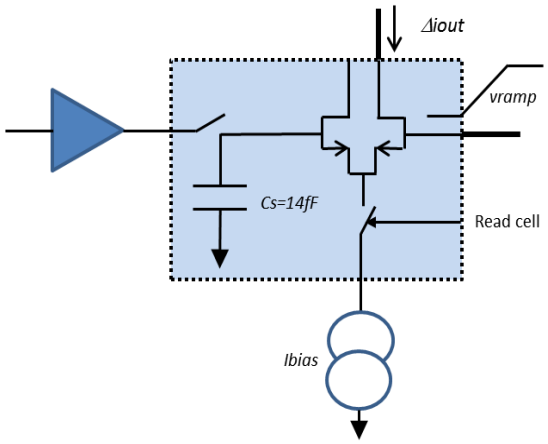
- Dynamic distorsion of the signal may be seen as noise.
  - Systematic non linearities:
    - Switches(Q injection), amplifiers: can eventually be calibrated and corrected.
  - Bandwidth dependency:
    - along the SCA (bus resistances): problem for long SCAs.
    - With the amplitude:
      - Switch non linearities (Ron)
      - Slew rate.
  - Dependency of the sampling time with the signal level.



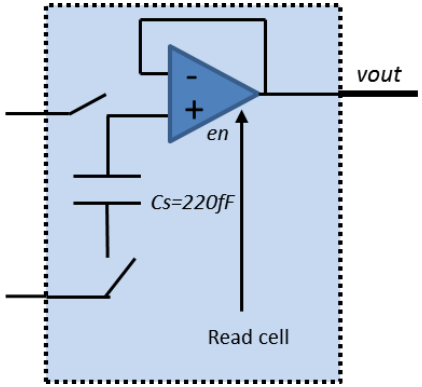
IN ADC datasheets: all this is included in the ENOB (together with jitter)

Intrisic Noise in SCAs

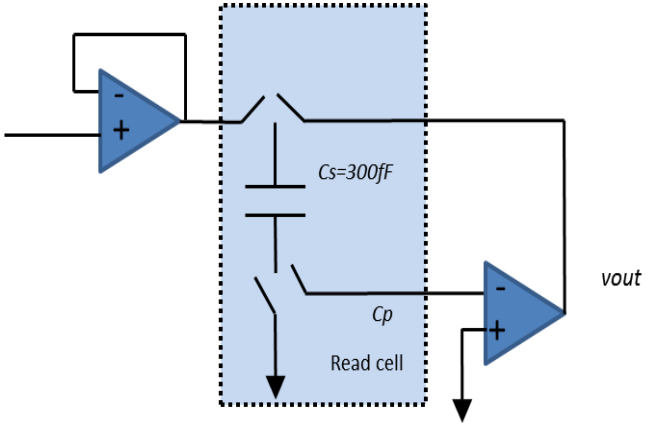
- Very architecture dependent
- 3 very different designs developed in the comunity
- But Common features/rules are existing.



« Target »:
Buffered SH
Wilkinson Readout
Very Small Cs

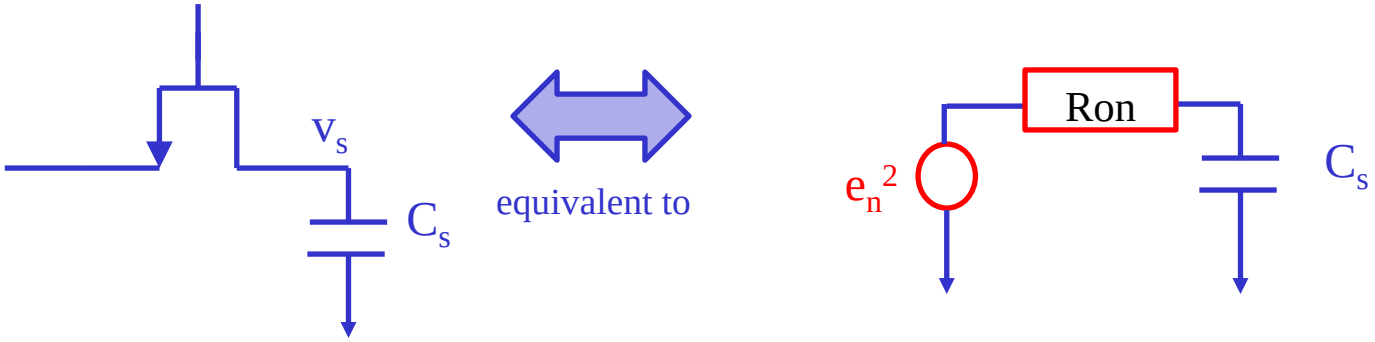


« DRS »:
Unbuffered diff SH
Closed Loop Follower readout.



« SAM »:
Buffered SH
Flip around readout
Fully differential

kTC or sampling noise when switching with MOS



When integrating the noise over the noise BW:

$\Rightarrow \langle V_s \rangle^2 = 4 .\gamma. k.T. R_{on.}B_N$ if 1/f is neglected

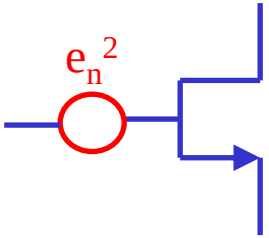
With Noise Bandwidth $B_N = \pi/2$ BW$= 1/(4.R_{ON.}C_s)$

$$\Rightarrow \mathbf{\langle V_s \rangle^2 = \gamma. k.T/C \text{ sampled on } C_s}$$

It is often reduced to kT/C

1/f noise contribution very complicated, mainly independant on C_s and often neglected . Is it sill true for deep submicron ?

Noise in CMOS technologies



When referred to input

en: Noise spectral density $e_n^2 = \frac{4kT\gamma}{g_m} + \frac{K_F}{C_{gs}f}$

Thermal noise:
γ = non ideality factor >=2/3
gm : transconductance scales as:
W/L and $I_D^{1/2}$ in strong inversion
I_D in weak inversion

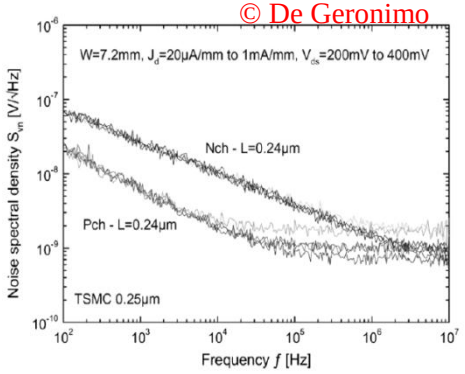
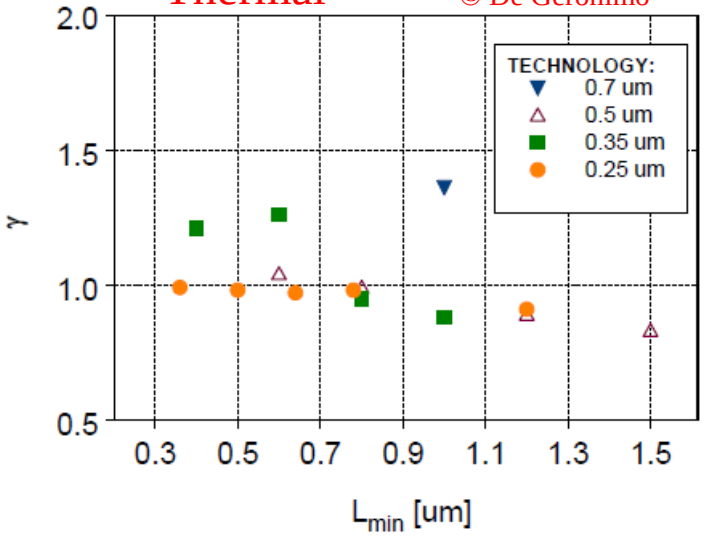


Fig. 12. Measured equivalent input noise spectra for n- and p-channel devices with minimum L and different J_d in TSMC 0.25 µm.

Flicker Noise: main source @ low frequency
~ independent of ID
Scales as (area)-1
Extends to few MHz in modern CMOS

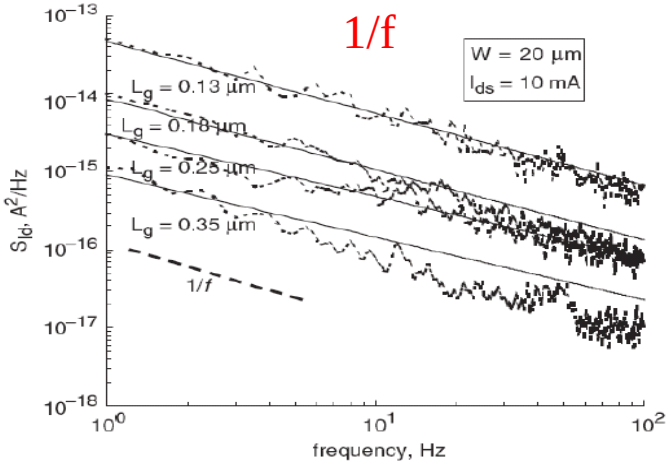
Effect of Technology scaling

Thermal



No dramatic degradation of γ with scale down

1/f



- High dependance with process details
- larger Kf when scaling down
- Degradation in time reported.

Intrinsic SCA Electronics noise: Quadratic sum of 4 terms

- **Input Buffer noise (if exists):**
  - $\sigma_{BUF} = e_n \cdot (\pi/2\ OBW)^{1/2}$

  e_n is the noise voltage density of the input pair, scales as $g_m^{1/2}$ ie $Id^{-1/4}$
  - σ_{BUF} =150µV rms/ 450MHz BW in SAMLONG (en= 4nV/ √ Hz)

- **Sampling noise** $\sigma_{kTC} = (kT/C_S)^{1/2}$ = noise floor of the SCA.

  => obvious tradeoff between noise and BW

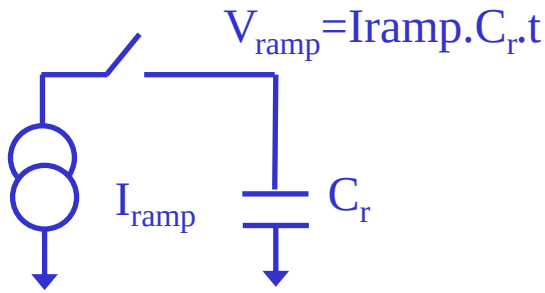
	Target	DRS4	SAM(LONG)
Cs (fF)	14	250	300
σ_{kTC} (µV rms)	540	130	120

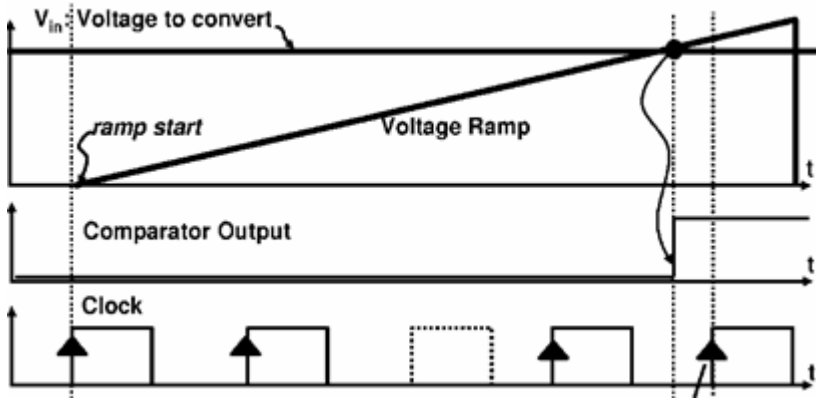
- **Output Mux or output buffer** (if exists):
  - Mainly OPAMP used as voltage follower.
  - Scales as 1/ √ gm = $Id^{-1/4}$ and as $(OBW)^{1/2}$ (output BW, can be decreased if lower speed readout).
  - 80µV rms in SAMLONG (20MHz mulitplexing).

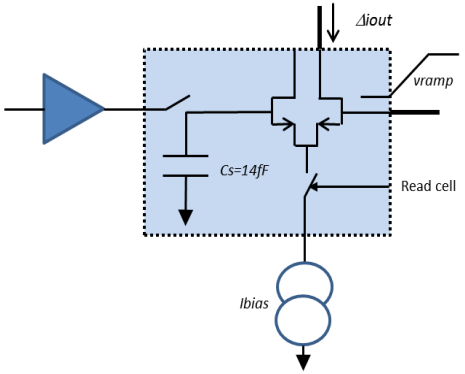
- **Readout noise**. See next slide.

ALL THESE CONTRIBUTIONS ARE MULITPLIED BY 2 fo diff. operation.

SCA ReadOut Noise: Wilkinson Readout







- Ramp noise

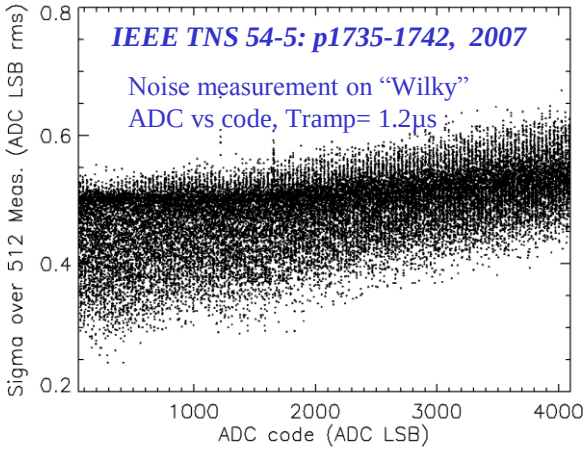
$$\sigma_{Ramp}^2 = (i_n^2/2 \,.\, t + K^2 K_f \,.\, t^2 \,)/C_r^{\,2})$$

i_n^2 is the thermal noise density of the current source (scales as gm or $I_{ramp}^{1/2}$)

K_F is the flicker noise coefficient, K is a constant.

⇒ Fast conversion is favorable.

⇒ Sigma scales as $1/C_r^{3/4}$ (thermal) or $1/C_r$ (1/f)

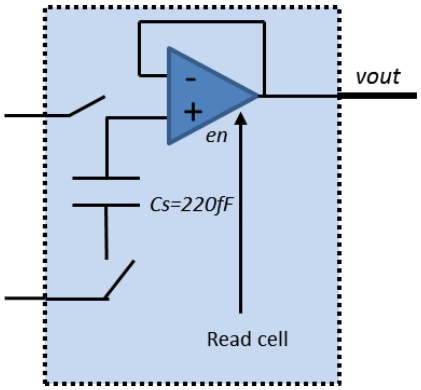


- Comparator noise.

Highly depend on the structure.

For a given speed σ_{comp}^2 scales as 1/gm of the input pair.

SCA ReadOut Noise: Follower readout



- Unity gain OTA or OPA

  If well designed (negligible 2nd stage noise).

$$\sigma_{Fol} = e_n \cdot (\pi/2\ OBW)^{1/2}$$

with e_n scaling as $1/\sqrt{g_m}$ (ie $1/ID^{1/4}$) and $1/(W/L)^{1/2}$ of the input MOS pair
one OTA/cell => transistor size limited

  - If not set externally OBW is proportional to gm / Cc

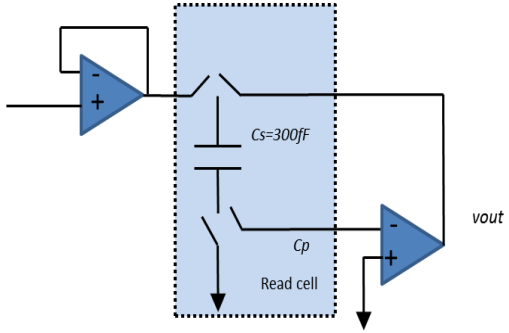
    $\Rightarrow \sigma_{Fol}$ becomes independent on g_m

  - If set externally: this contribution can be decreased if the RO frequency is decreased.

- For the same power consumption the noise of a MOS used as a source follower is better by 2 or more (for the same area used).

:

SCA ReadOut Noise: Flip around Readout



Unfortunately this configuration amplify the OPAMP noise:

$$\sigma_{FA1} = e_n \cdot (C_P + C_S / C_S) \cdot (\pi/2\ OBW)^{1/2}$$

With e_n = input refered noise density of the amplifier

scales as 1/gm.

can be minimized by increasing input transistor size (only one ampli/ channel)

=> C_p must be minimized by design/layout and C_s maximized.

=> for long SCA the noise becomes proportional to the SCA length.

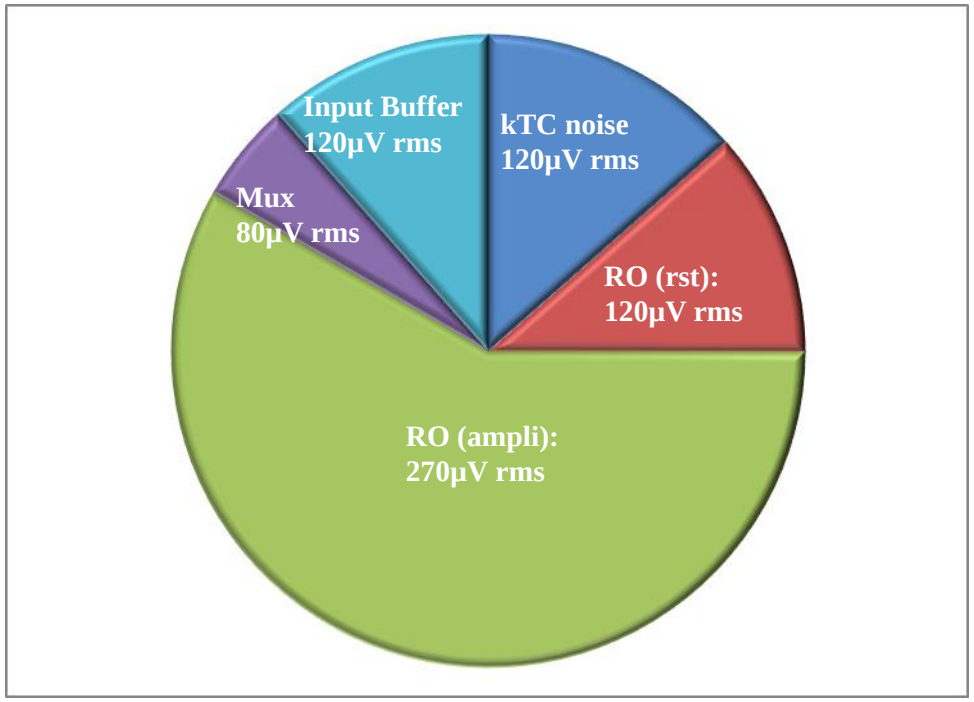
=> can be decreased if OBW is limited => slower readout.

Before reading Cs, Cp must be reset:

=> extra contribution $\sigma_{FA2} = (kT/C_S)^{1/2}$ with the most efficient reset scheme

On SAMLONG RO noise contribution is σ_{FA1} = 270µV rms (20MHz ReadOut)

Exemple: of the « Intrinsic Noise » contributions for SAMLONG



Total : 350µV (single ended) => 500µV rms differential

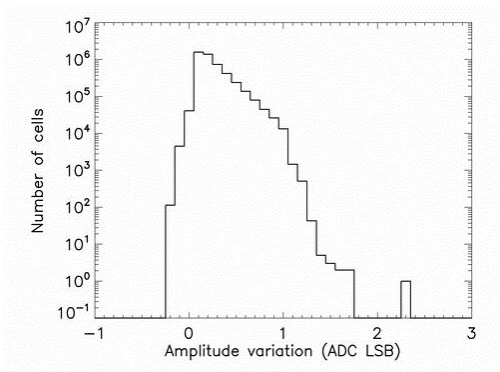
Clearly dominated by ReadOut contribution:
Price to pay for a “robust” readout.

Another possible noise contribution

- Switches Leakage currents are discharging Cs:

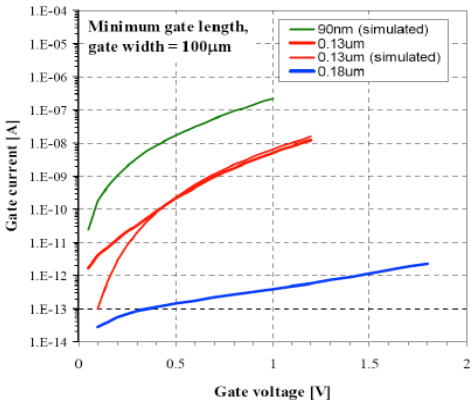
  => voltage drop depending on time between W and R.

- Not an issue with old technologies:

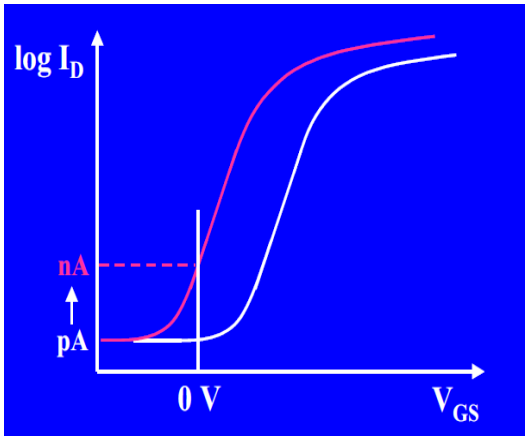


AFTER Chip (T2K TPC) AMS 0.35µm
Distribution of the voltage on 120 chips * 65000 cells
drop after 2 ms.
1 LSB = 0.5mV => 55fA

- Can become a problem in deep submicron:



Gate tuneling curent



Low VT + Low weak inversion slope

Use of True Differential signaling ?

- Pros:
  - Max signal doubled.
  - SCA noise increased by √2

  } S/N increased by √2

  - Less distorsion (even harmonics cancelled)
  - D/A coupling rejected
  - Good PSRR
  - Leakage effect compensation.
  - Massively adopted in industry

- Cons:
  - Power consumption increase.
  - SCA surface doubled.
  - With a similar increase, you could increase Cs and theoretically improve theS/N by more than √2
  - Detector signal are often single ended => need for an interface element

Use of OPAMP or single-ended structure ?

- In the first fast SCA we designed (ARS):
  - The amplifiers were single ended.
  - The structure was not differential.
- REAL S/N was limited to ~8-9 bits because of temperature stability of gain and baseline spread (no correction performed at all)
  - => All this has been improved by the use of closed loop OPAMP.

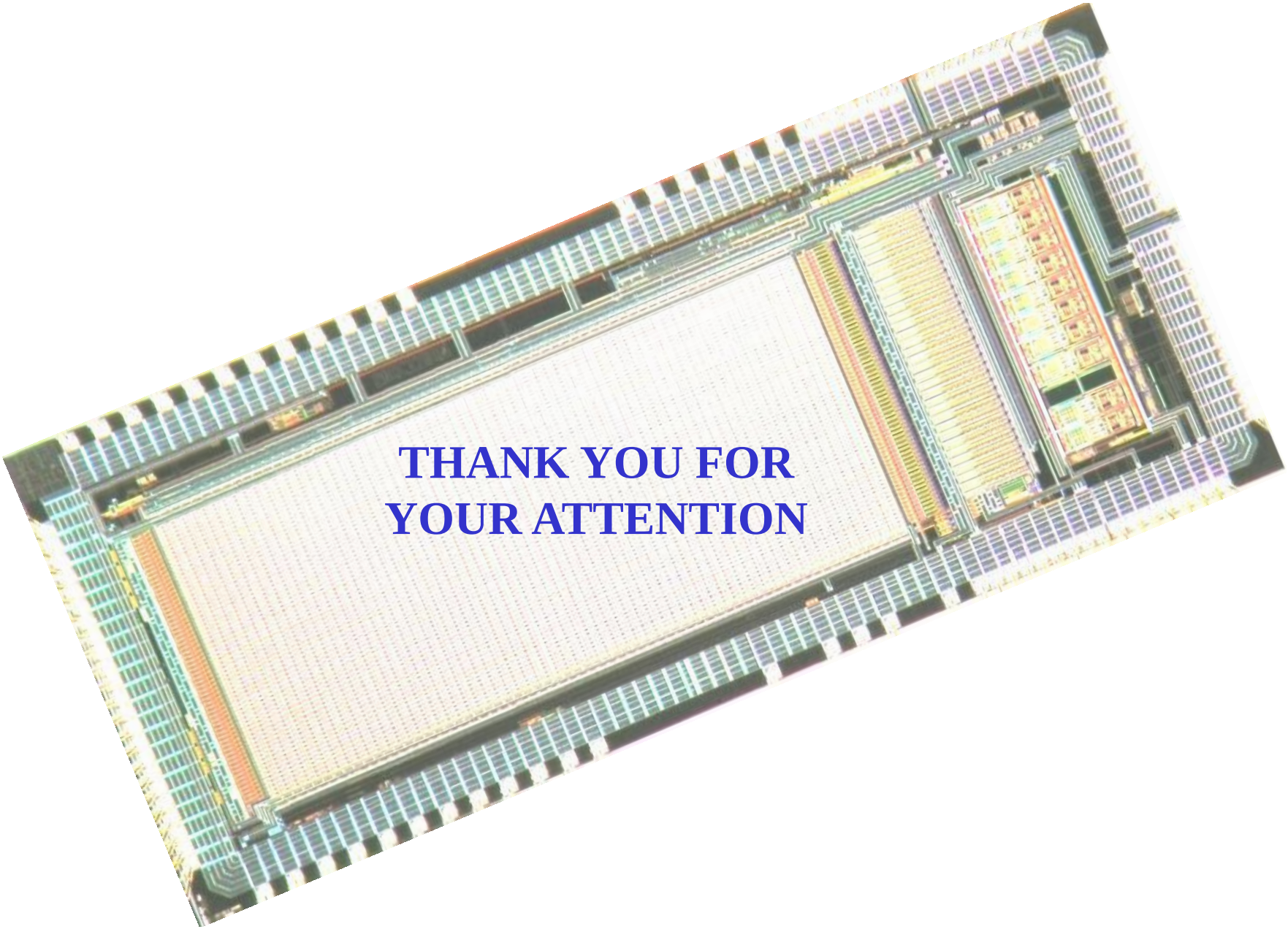
- But for the same power consumption, the noise of an OPAMP is more than $\sqrt{2}$ larger than for a single ended one.

- Modern technologies are offering NMOS with seperate wells

  => Good candidates for linear followers, power , area and speed efficient.

  => Used in the MDACs of several recently published 10-bit pipeline ADC designs.

  => Differential structure cancels spread and sensitivity to supplies and temperature .


THANK YOU FOR
YOUR ATTENTION