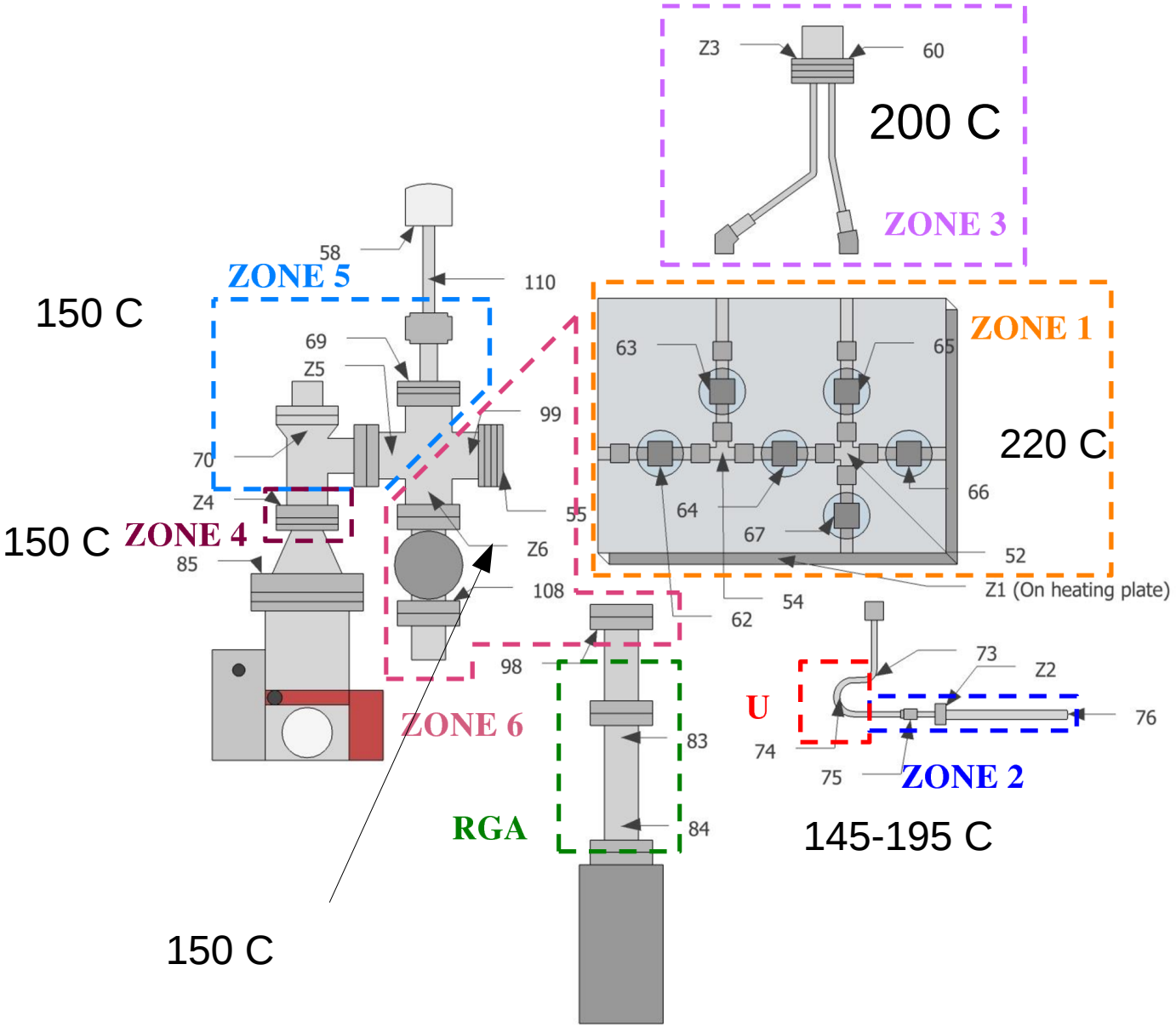
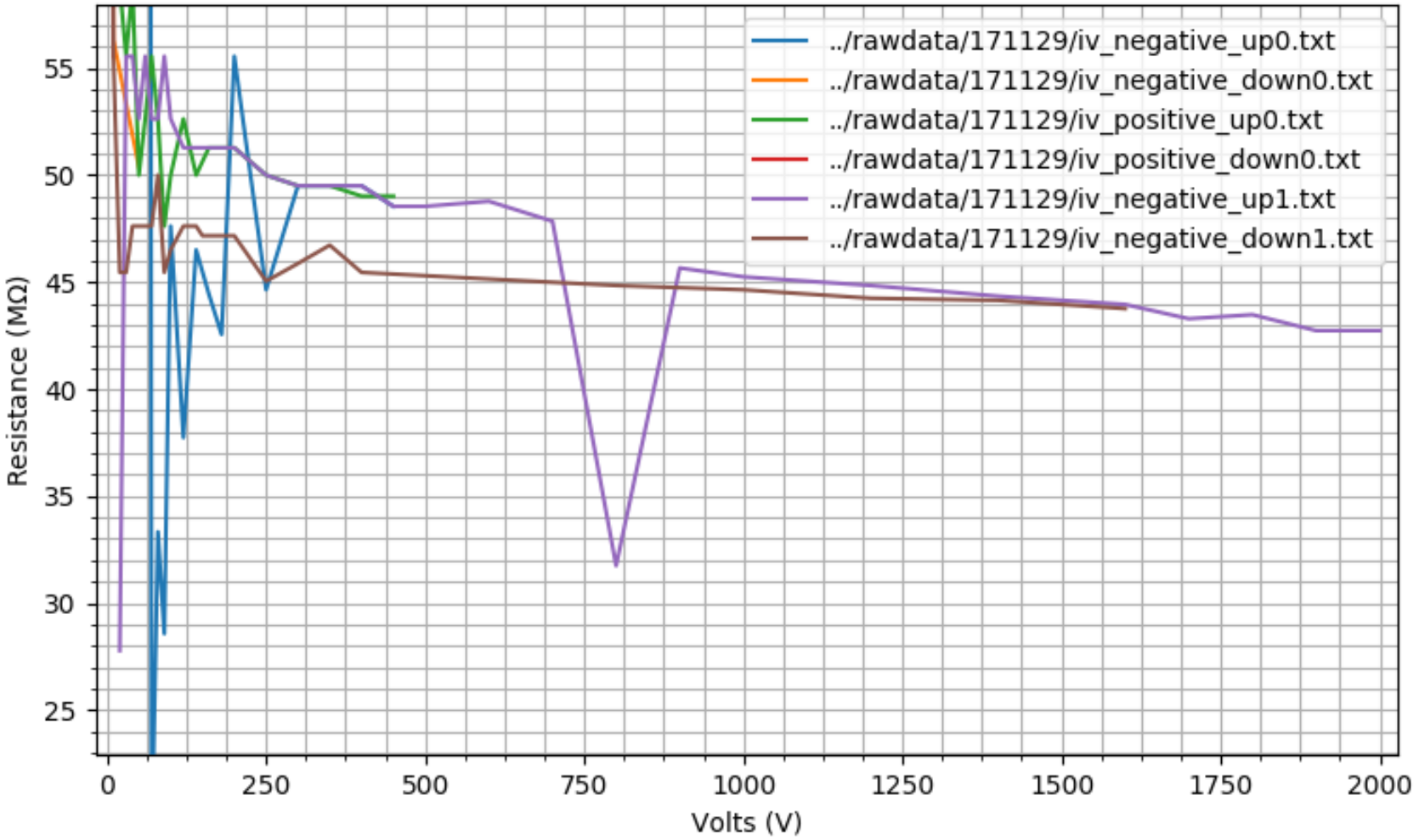
Detailed Steps From Tile 21

1) Adjust temperature of manifold to permit flow of cesium while minimizing outgassing
2) Measure I-V characteristic of tile
3) Scrub
4) Measure I-V characteristic of tile
5) Heat the tile to 120 C to permit flow of cesium and photocathode formation
6) Measure I-V characteristic of tile
7) Apply 120 V DC bias across tile
8) Admit cesium while measuring photosensitivity at 405 nm
9) Stop admitting cesium when?

Manifold Condition



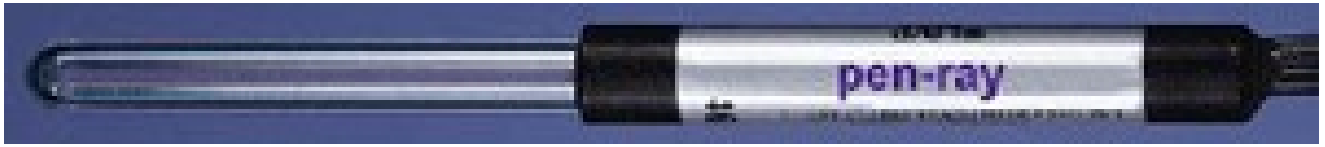
I-V Characteristic Before Scrubbing



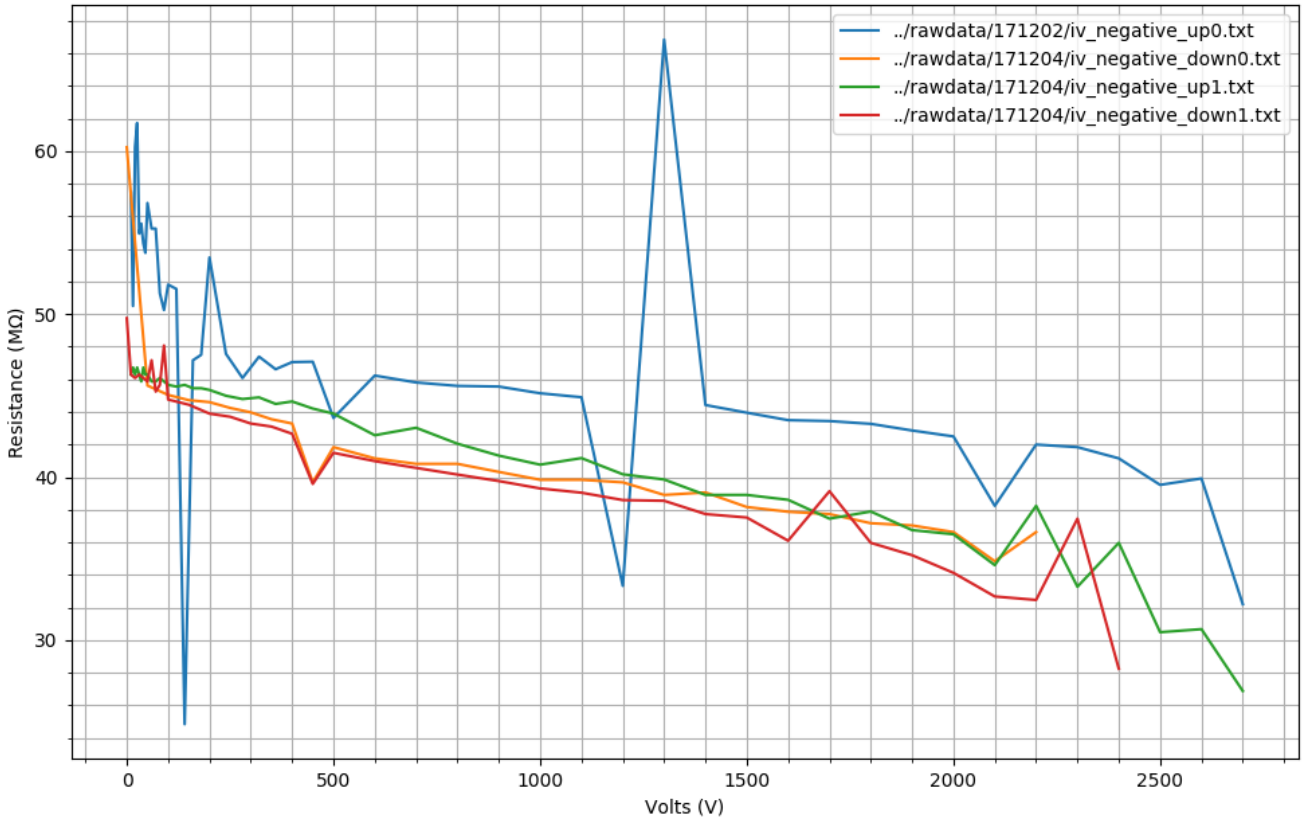
Plot shows dV/dI vs V

Scrub

- Illuminated tile with a small mercury vapor lamp while bias voltage was 1750 V
- Current draw was ~135 microamps, slightly decreasing with time
- Uniform illumination achieved by dithering lamp

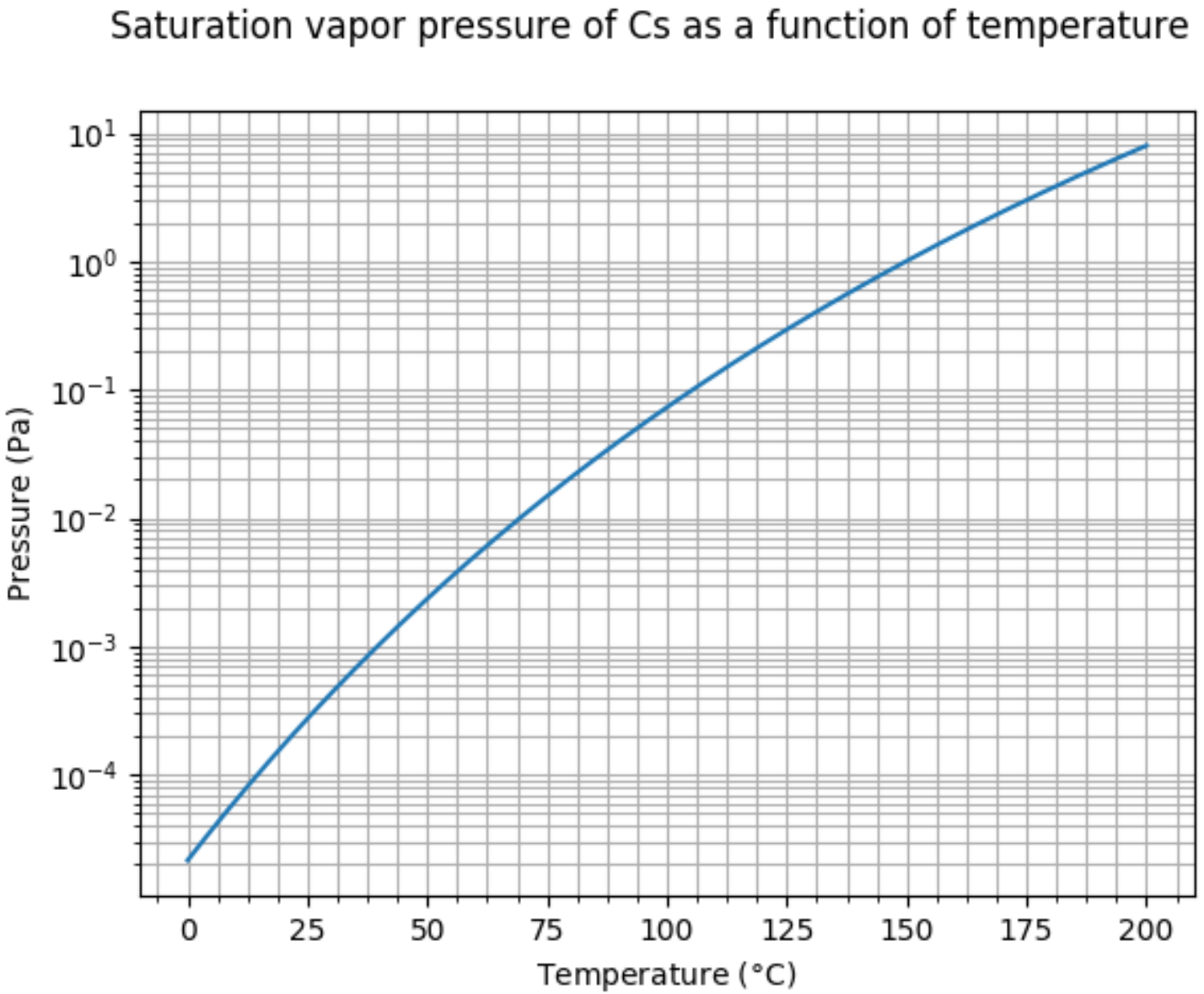


I-V Characteristic After Scrubbing



Slight drop in stack resistance was observed after scrubbing

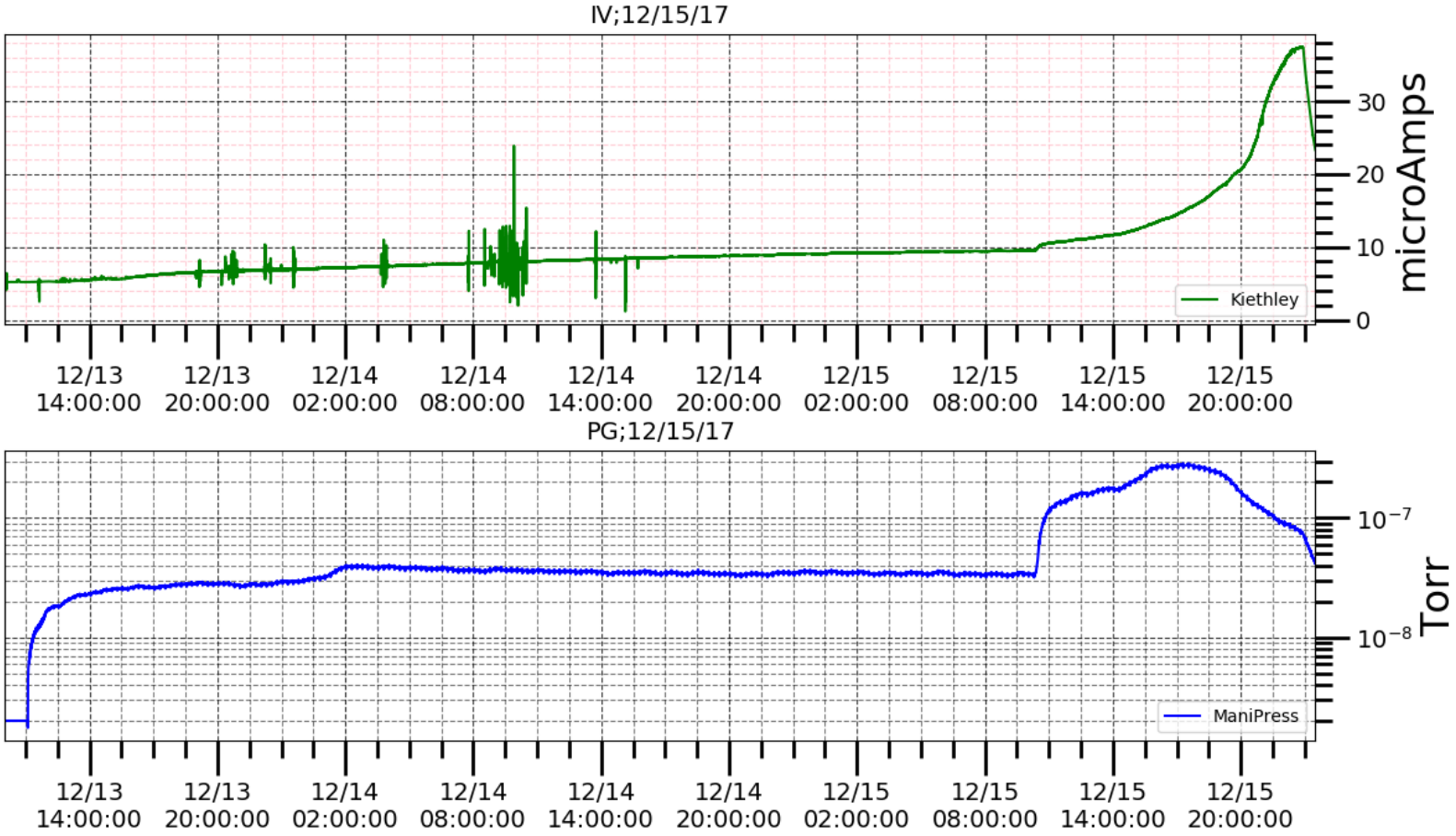
Heat tile to 115 C



I-V Characteristic With Tile Hot

- Stack resistance dropped from 45 to 24 MOhm
- Internal resistors known to have a much smaller temperature coefficient compared to MCPs
- I-V characteristic was thought to be useful for assessing the behavior of the MCPs while the tile was still hot
- Since then, we have learned that the internal resistors are degraded by Cs, so the stack resistance is less informative

Admit Cs


IV;12/15/17
Kiethley
microAmps
30
20
10
0
12/13 14:00:00
12/13 20:00:00
12/14 02:00:00
12/14 08:00:00
12/14 14:00:00
12/14 20:00:00
12/15 02:00:00
12/15 08:00:00
12/15 14:00:00
12/15 20:00:00
PG;12/15/17
ManiPress
Torr
10^{-7}
10^{-8}
12/13 14:00:00
12/13 20:00:00
12/14 02:00:00
12/14 08:00:00
12/14 14:00:00
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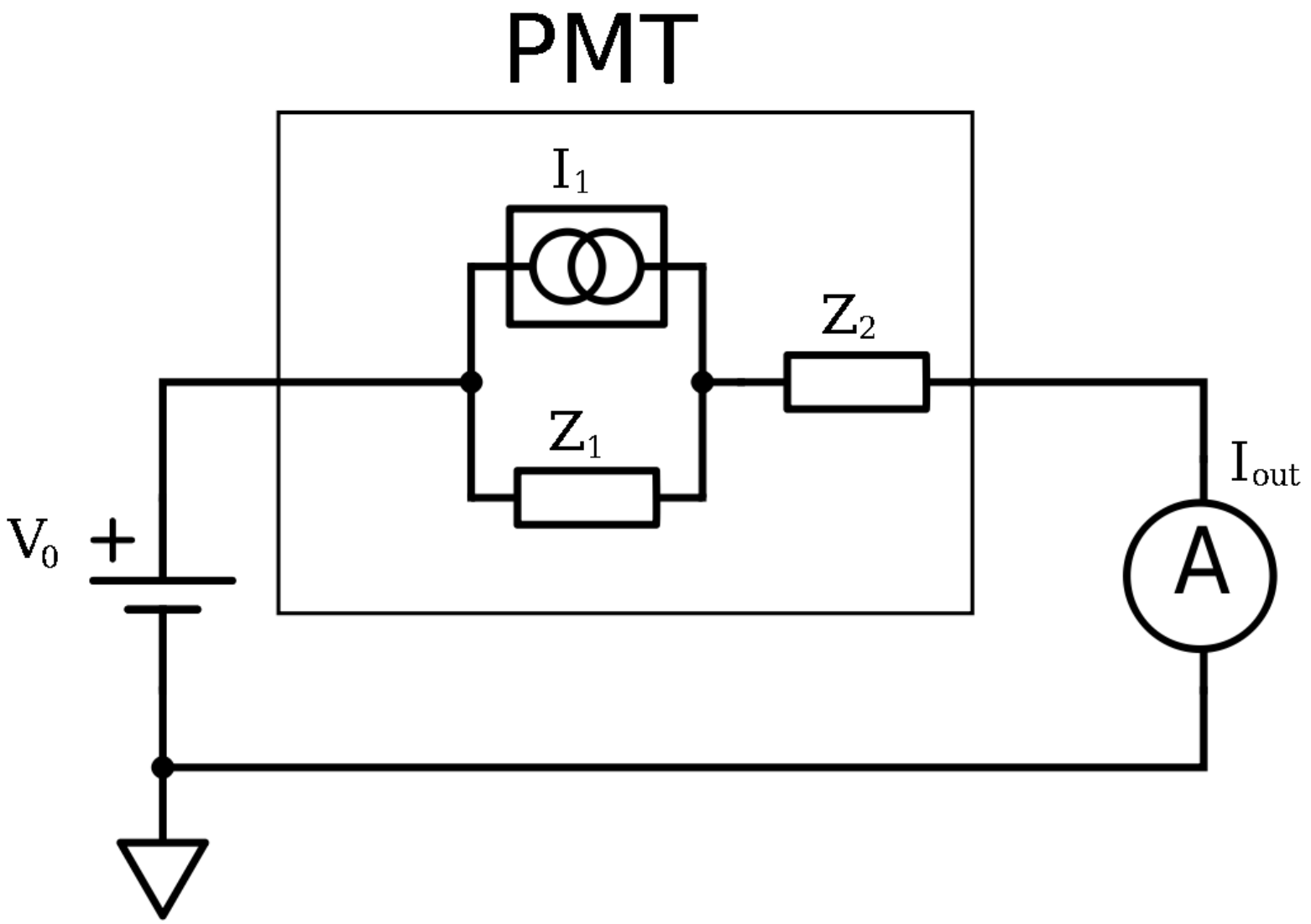
12/15 14:00:00
12/15 20:00:00

Resistive Divider Factor



Simple-minded Improvements to Tile 21 Procedure

- Use feedthroughs instead of internal resistors; we have tested the electrode scheme in Tile 23 and 24
- Measure QE of photocathode, since internal resistors no longer interfere
- Use distilled Cs in a copper tube for improved reliability of Cs flow
- Calculate/calibrate conductance to tile from Cs source and keep a Cs budget (estimate is ~5e-3 L/s)