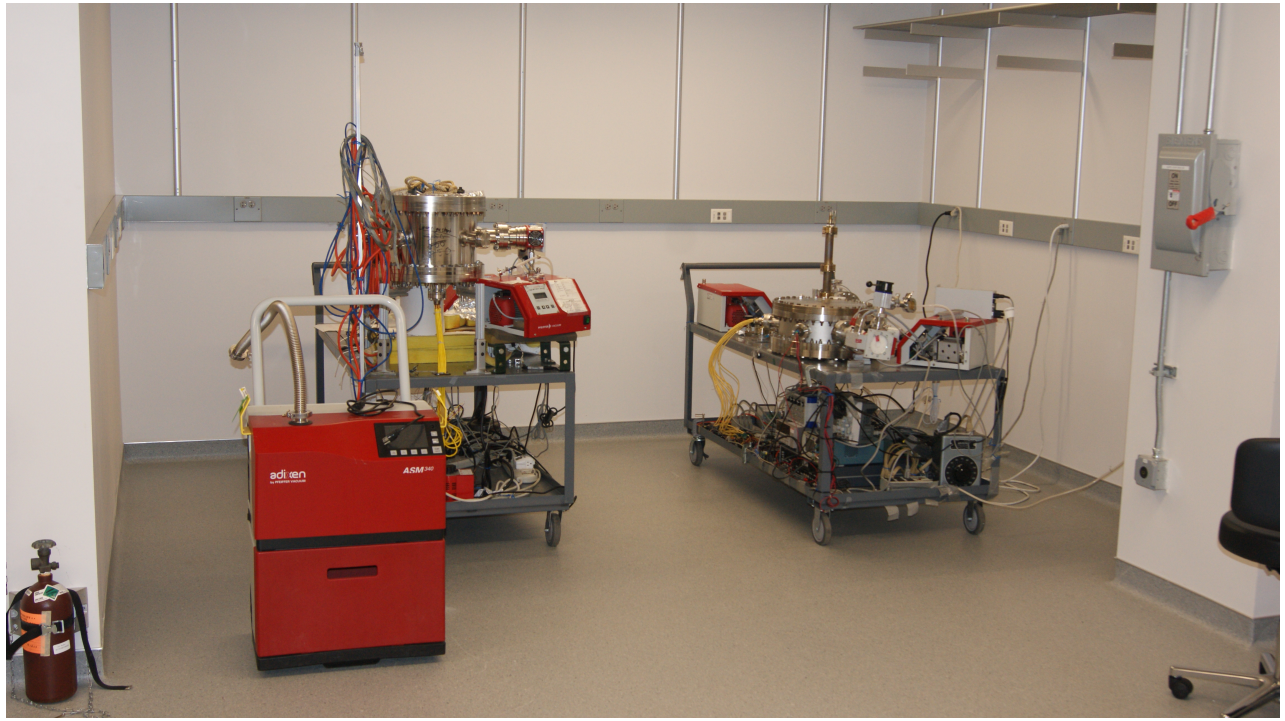
Problems solved and problems not-solved since the last GP review

Evan Angelico

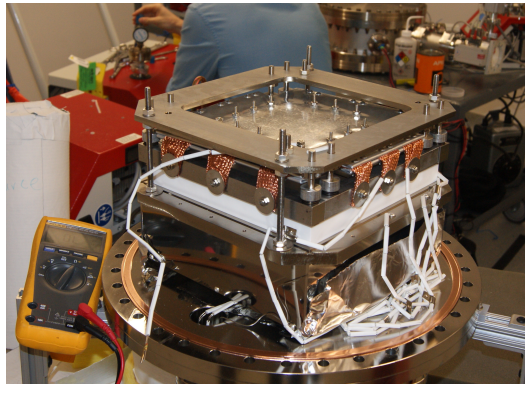


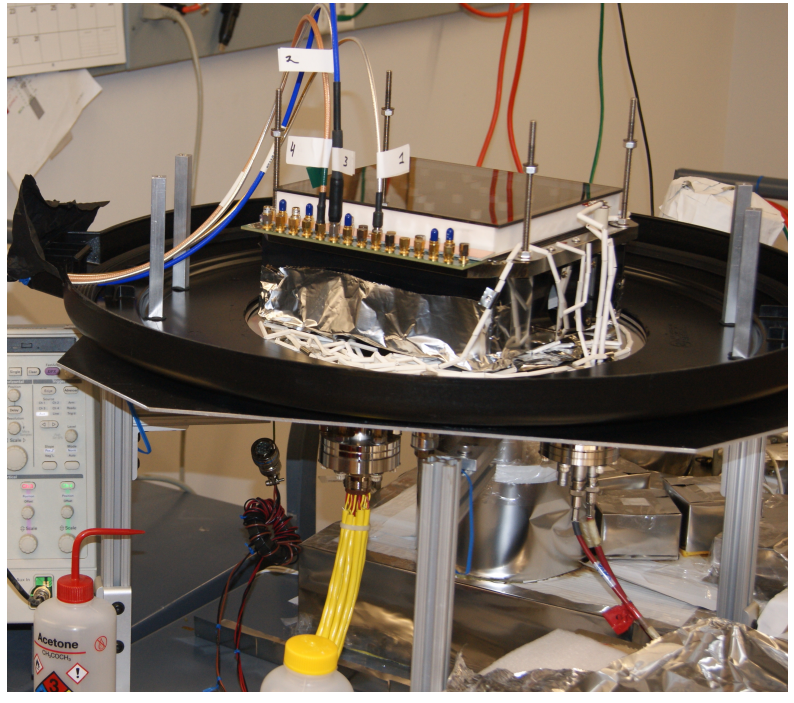
Improvements to procedure and facility upgrades

Improvements in procedure and facility upgrades

- Serious facility upgrade
  - Sinks, wet lab, fume hood, clean areas
  - Overhead crane
  - Margherita 4pi access, organization
  - Clean power
  - Regular mopping

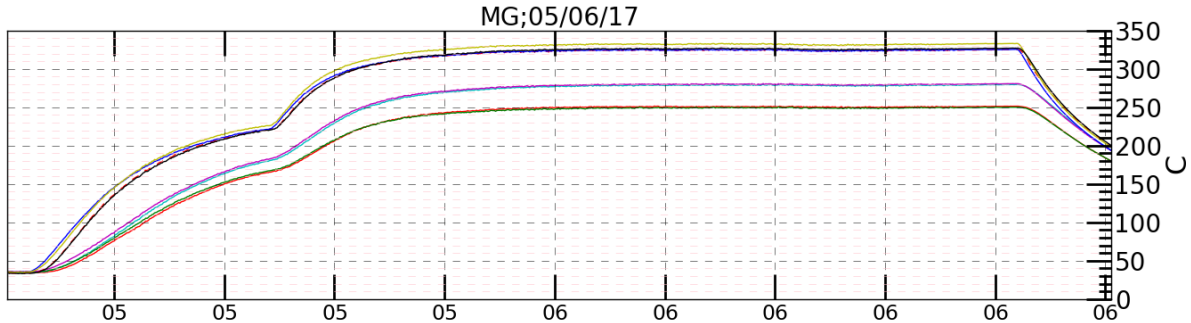
- Two Margherita facilities
  - Full side access to LAPPDs in fab.
  - Double tile fabrication throughput



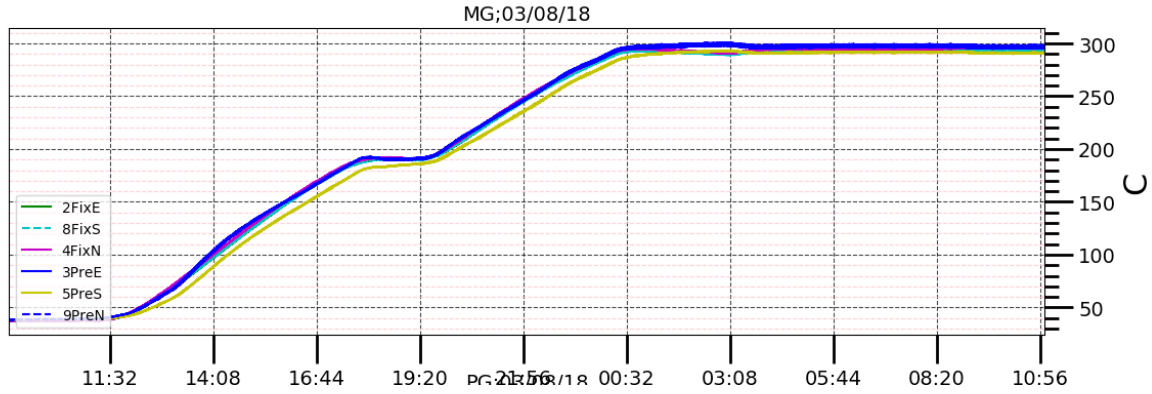


Improvements in procedure and facility upgrades

- In house Indium etching
- In house MCP baking
- <1 mil precision on stack height
- Quartz-tungsten lamps → NiCr heaters

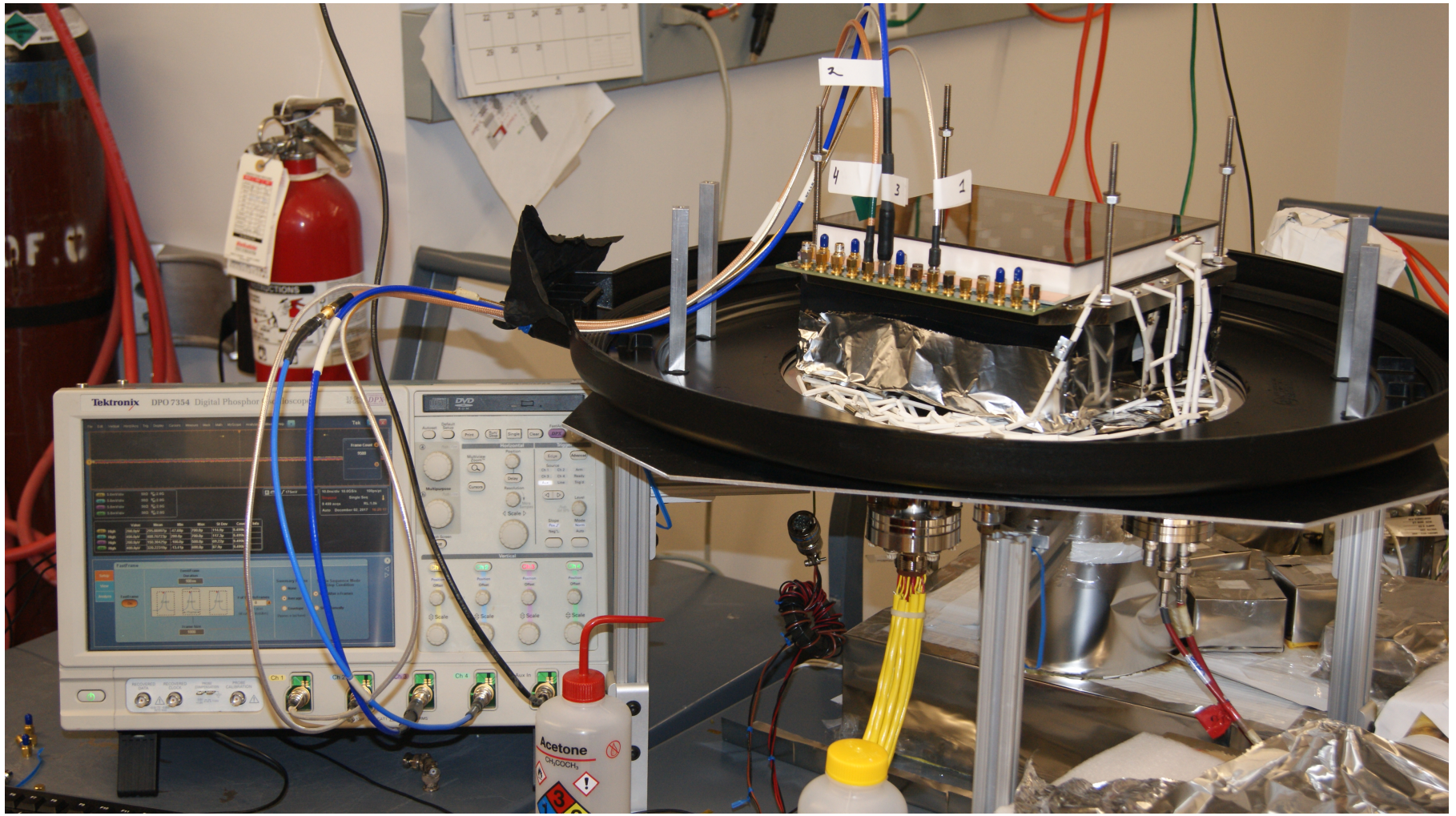


- Thermal uniformity of the LAPPD in production
  - Insulation and heater design a-la Eric
  - ~5 degree C spread between window and ba
  - Indium is uniform to 5C



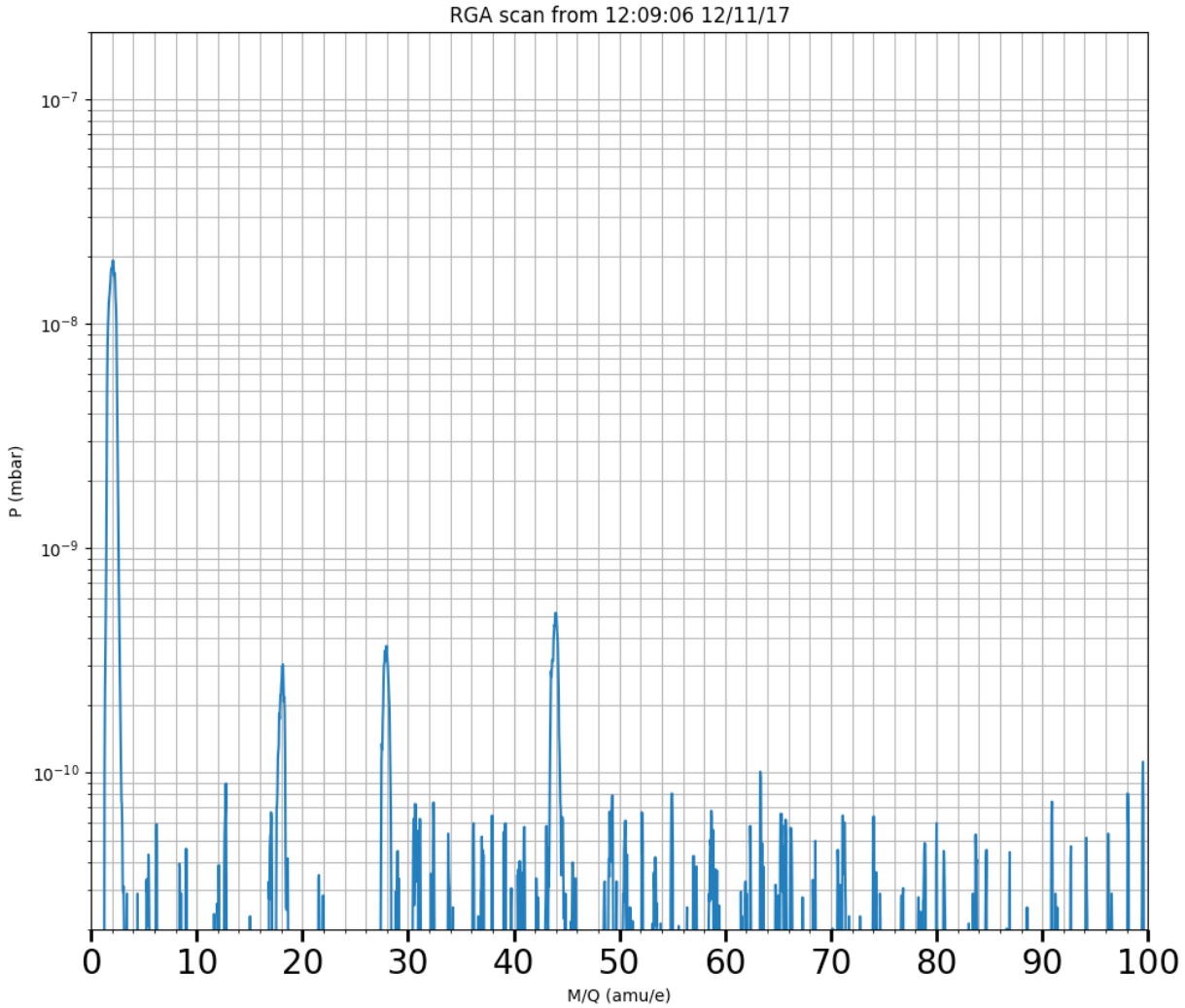
Improvements in procedure and facility upgrades

- In-situ pulse readout with 30 channels

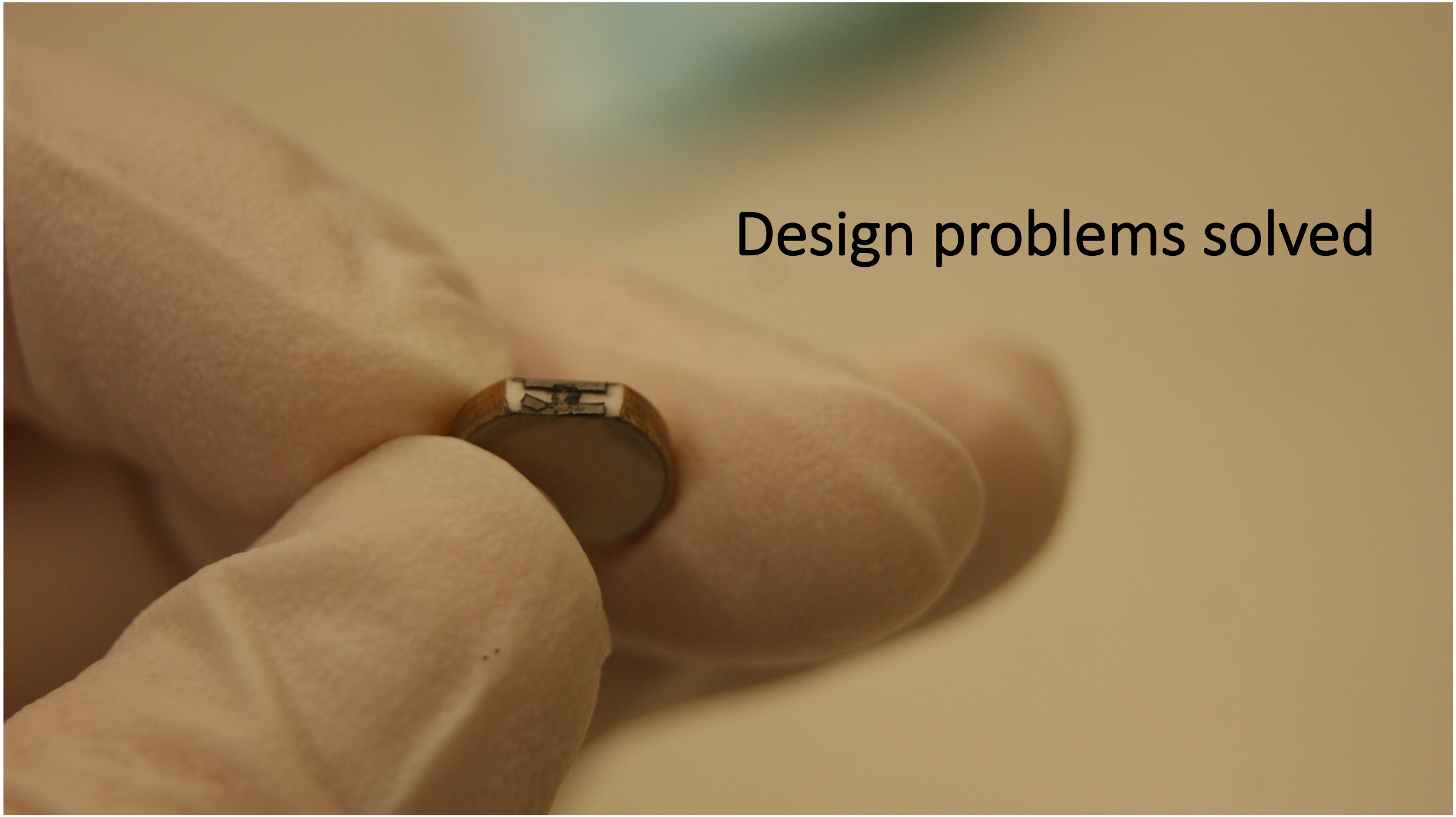


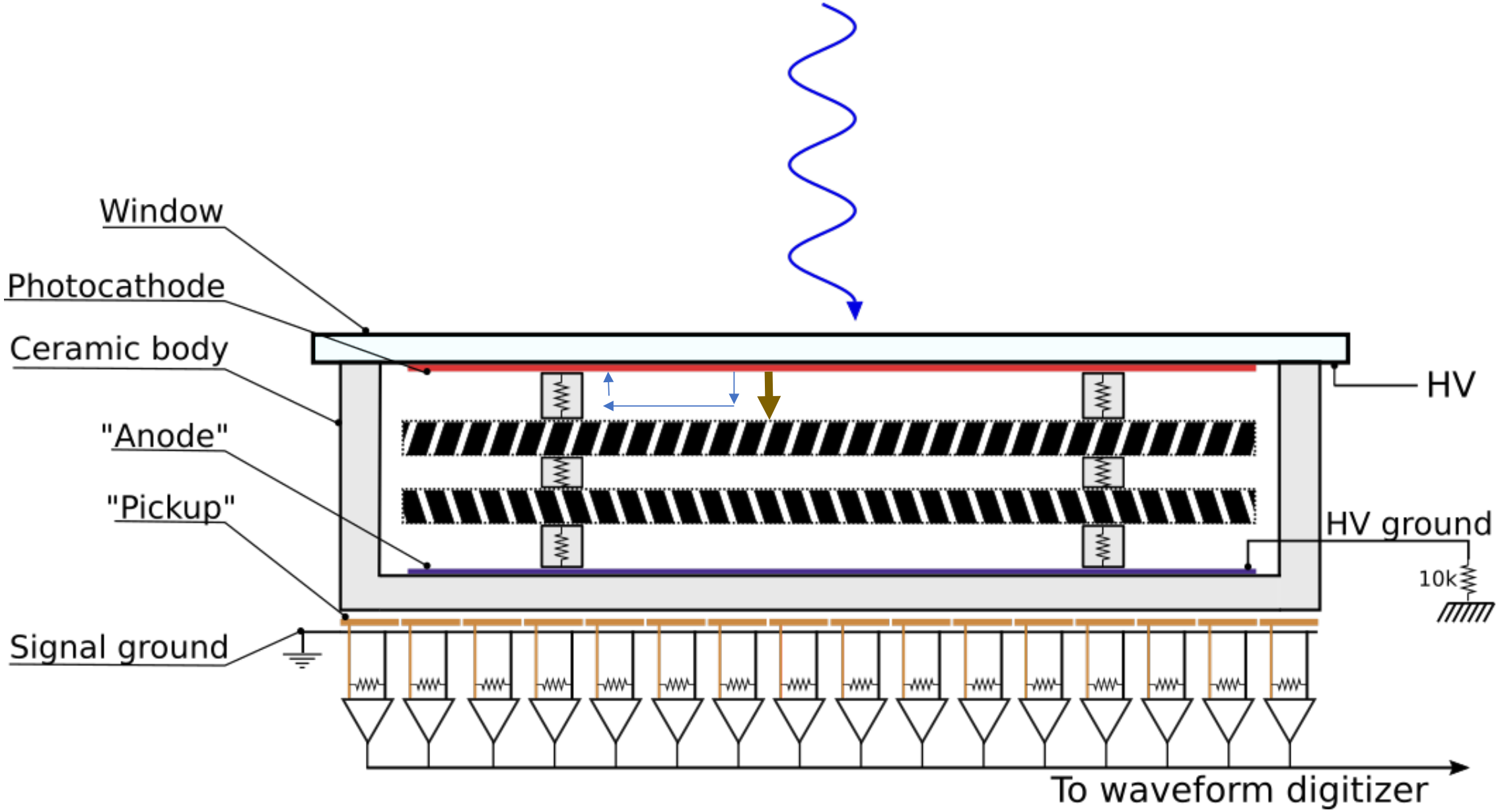
Improvements in procedure and facility upgrades

- Improved cleanliness of Cs manifold and temperature control



- Manifold pressure is below detection threshold (2e-9) at cesiation temperatures
- RGA filament dominates pressure (we now know how to degas it effectively)
- More in session 5

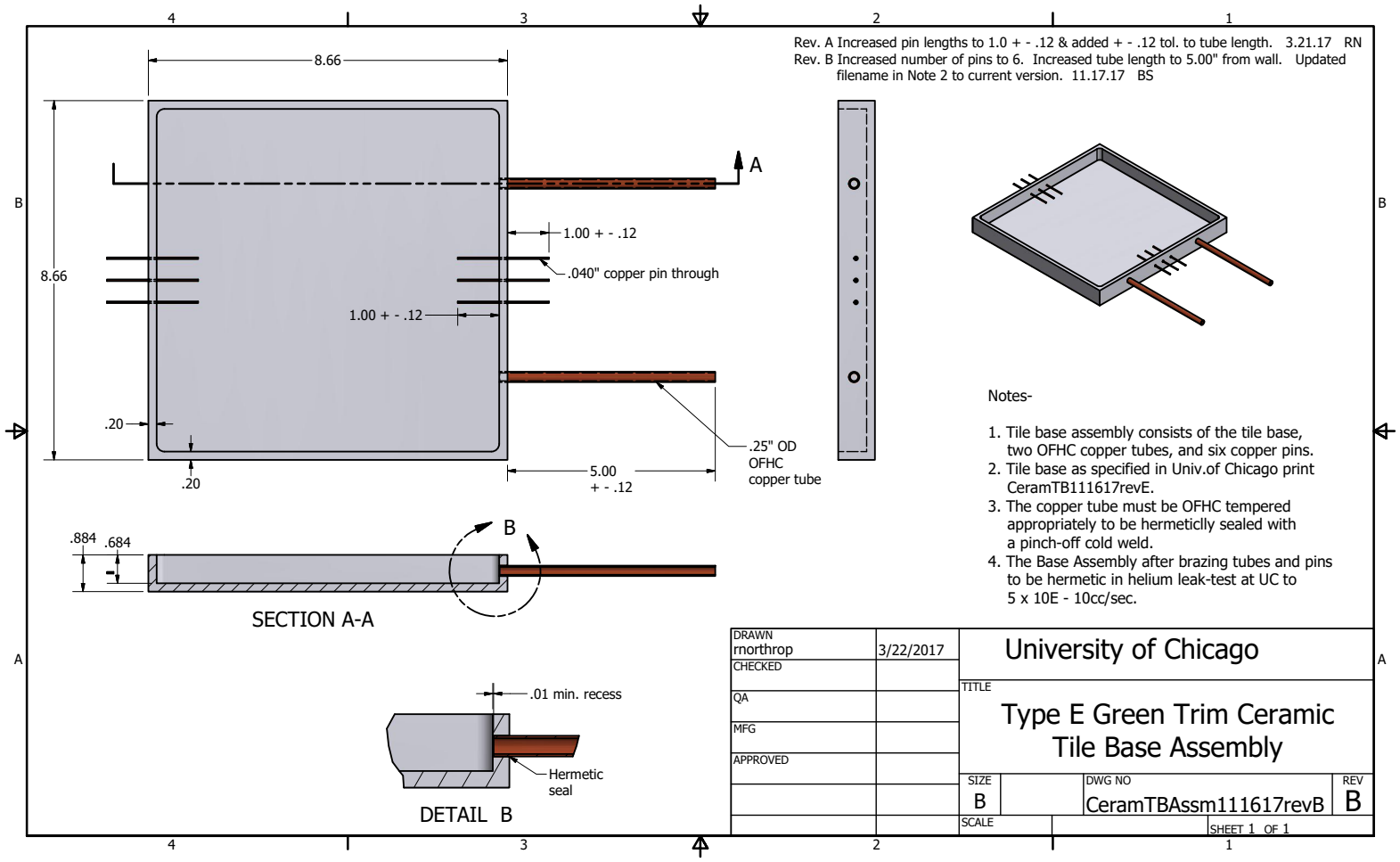

Design problems solved


Window
Photocathode
Ceramic body
"Anode"
"Pickup"
Signal ground
HV
HV ground
10k
To waveform digitizer

Design problems solved

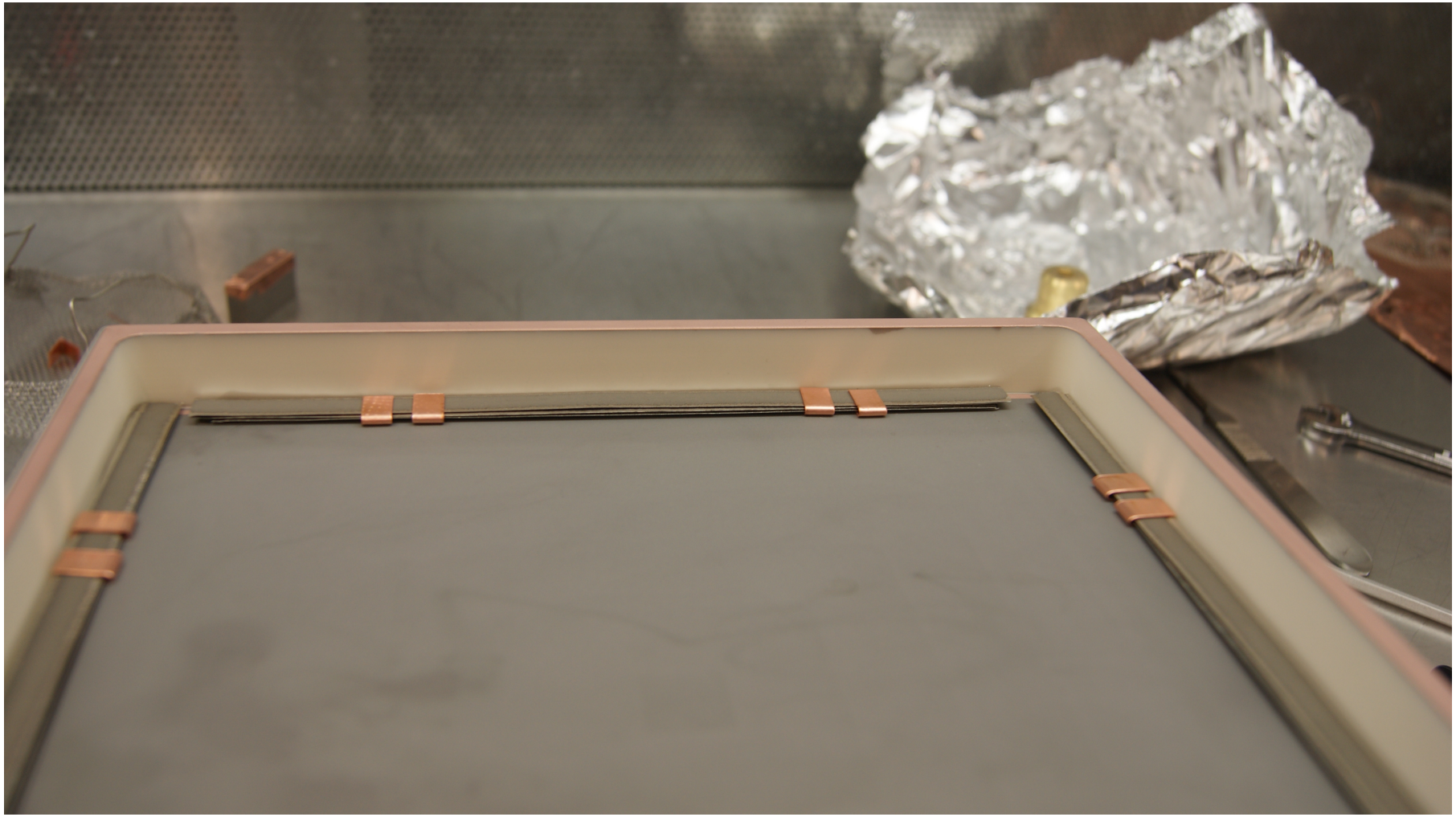
External voltage divider:

- Accurate QE measurement
- Optimize gap voltages for best timing
- Measure isolated MCP resistance during cesiation



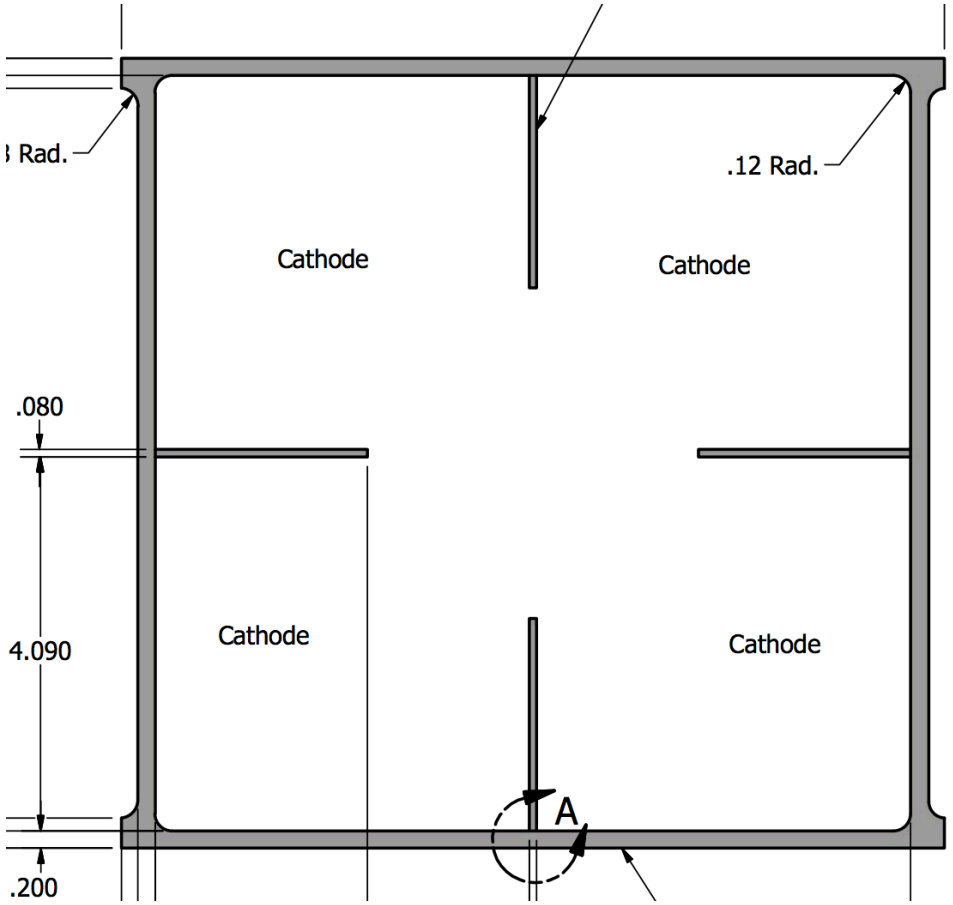
Design problems solved

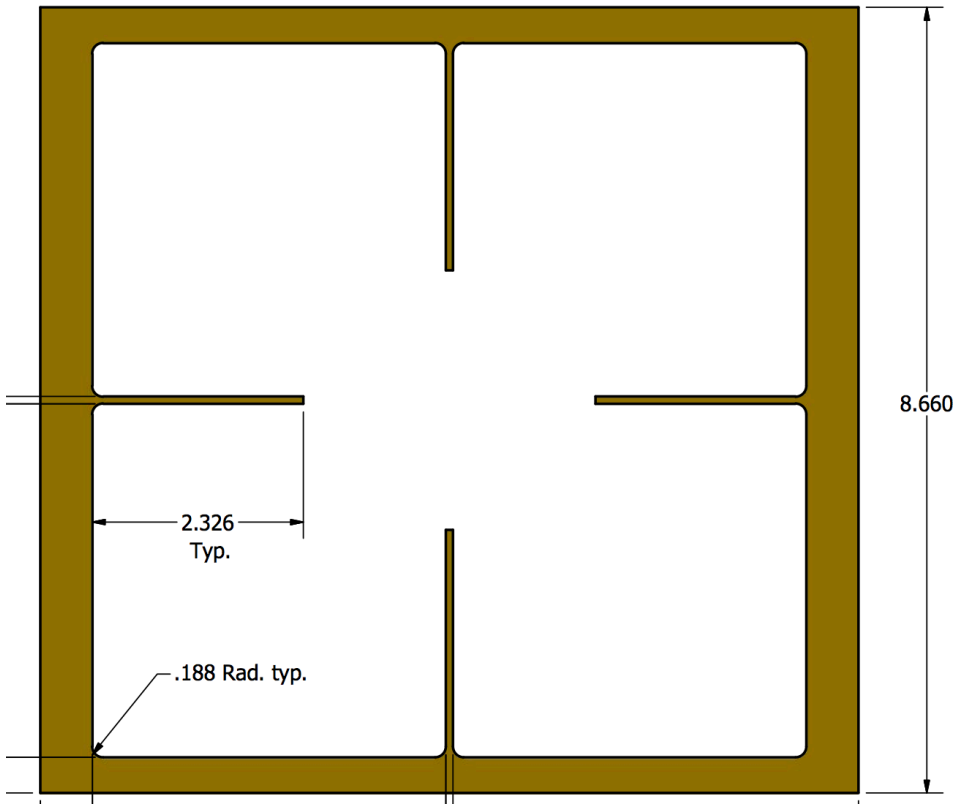
- Getter mounting, 10g of active material



Design problems solved

- Window metalization change
  - Indium wicking, loss of indium mass
  - Indium-Cesium mixture makes powder



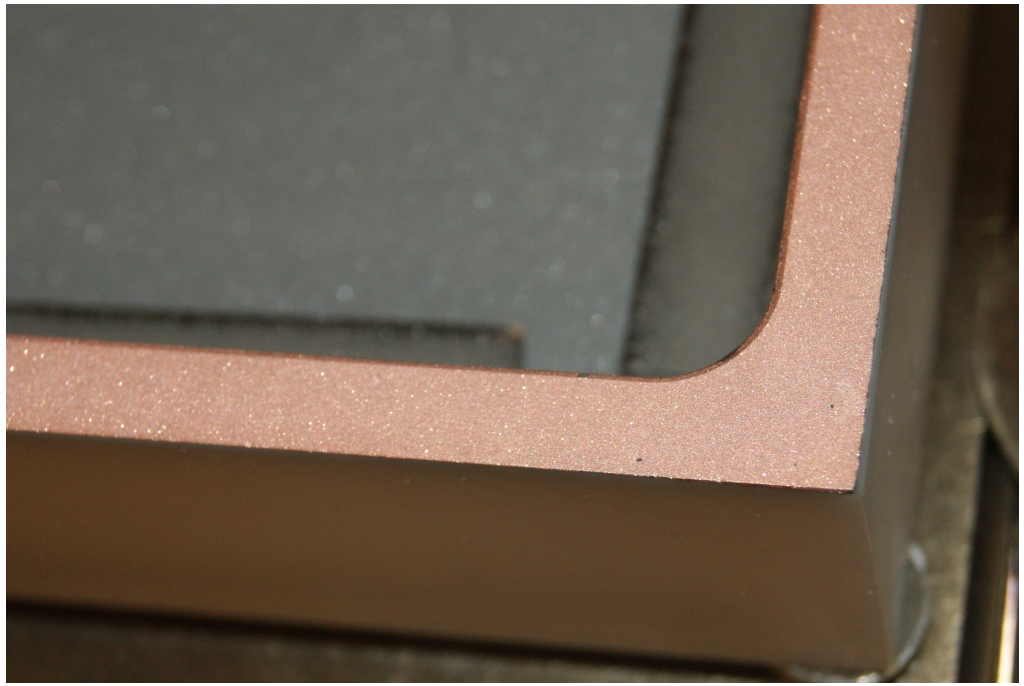


he tile, in crevices and on
n the window. It was col-
om the window, and flaked

Design problems solved

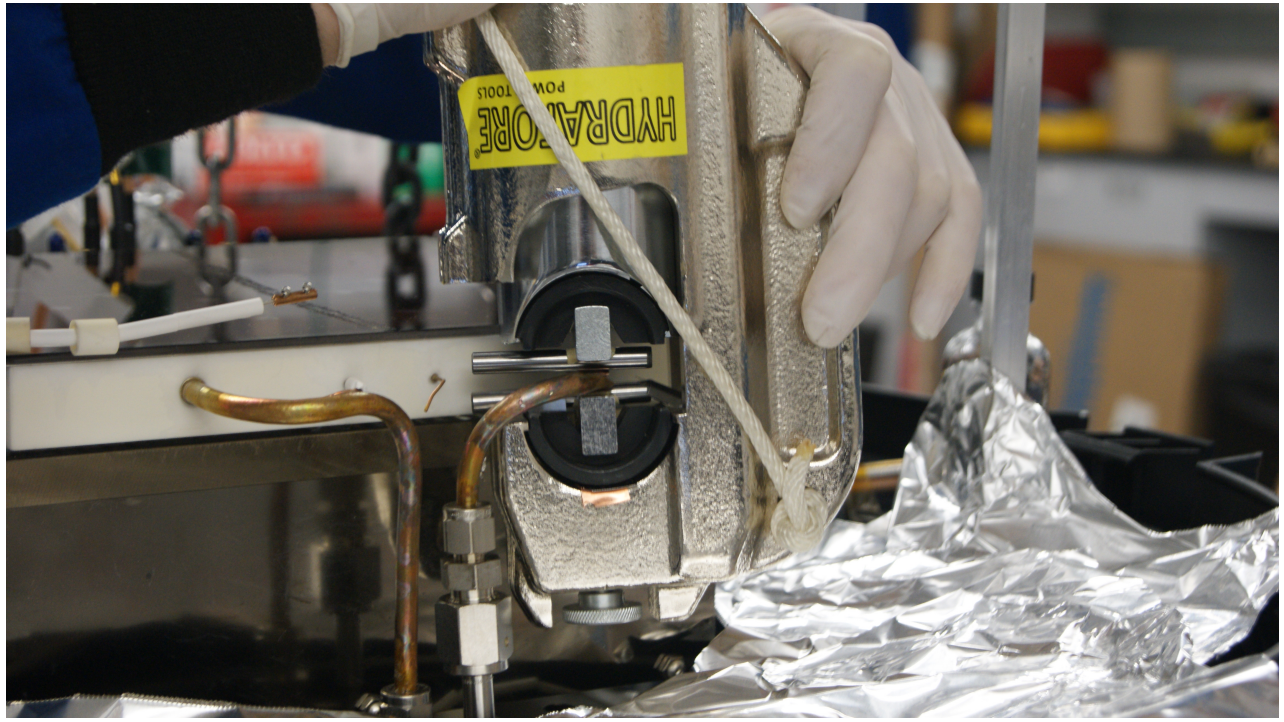
- Metalizing vendors
  - PURE metals

- Evaluating 4 ceramic vendors

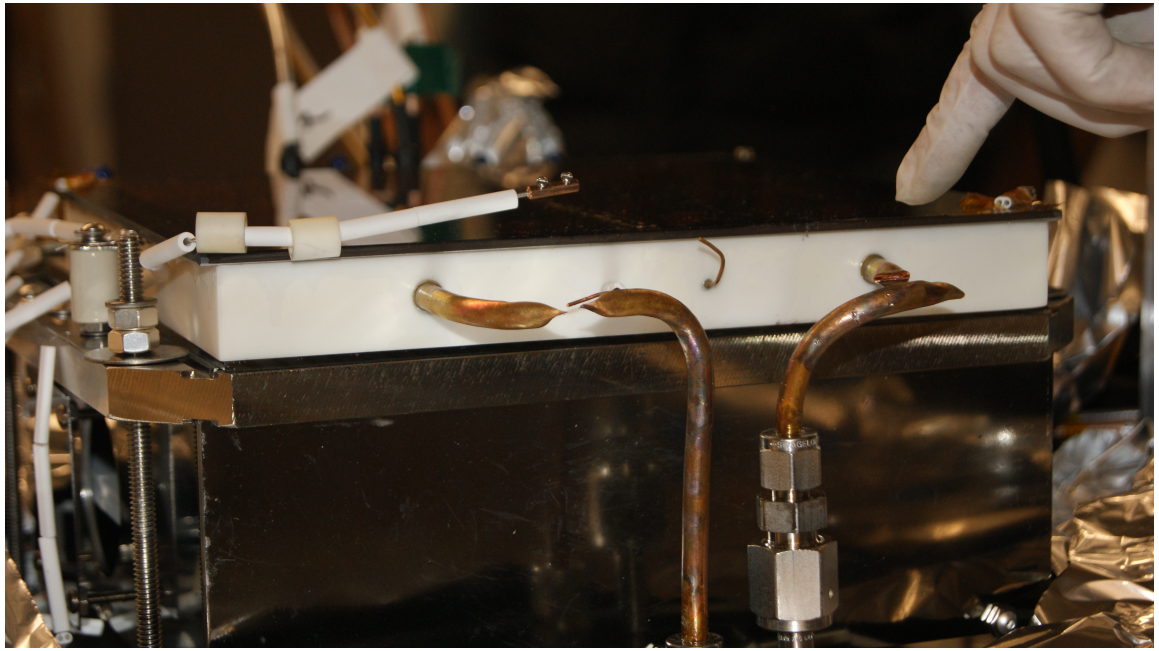


Design problems solved

- Copper tube pinch-off



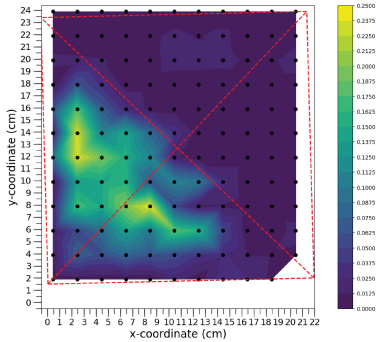
New tool to try out next time



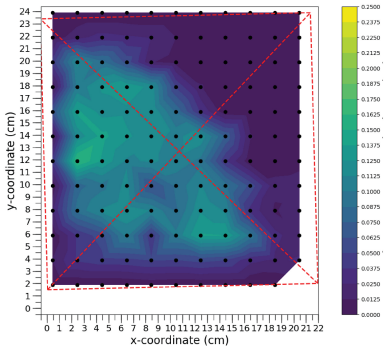
Tile 21 pulses!

Capacitive pickup, 30 strip-line readout

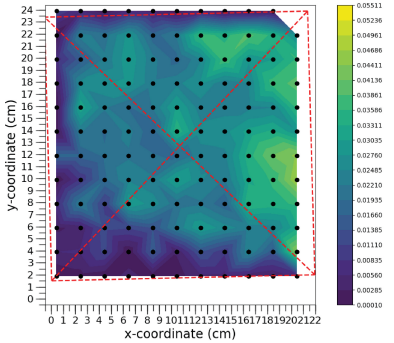
After 24 hours of cesiation

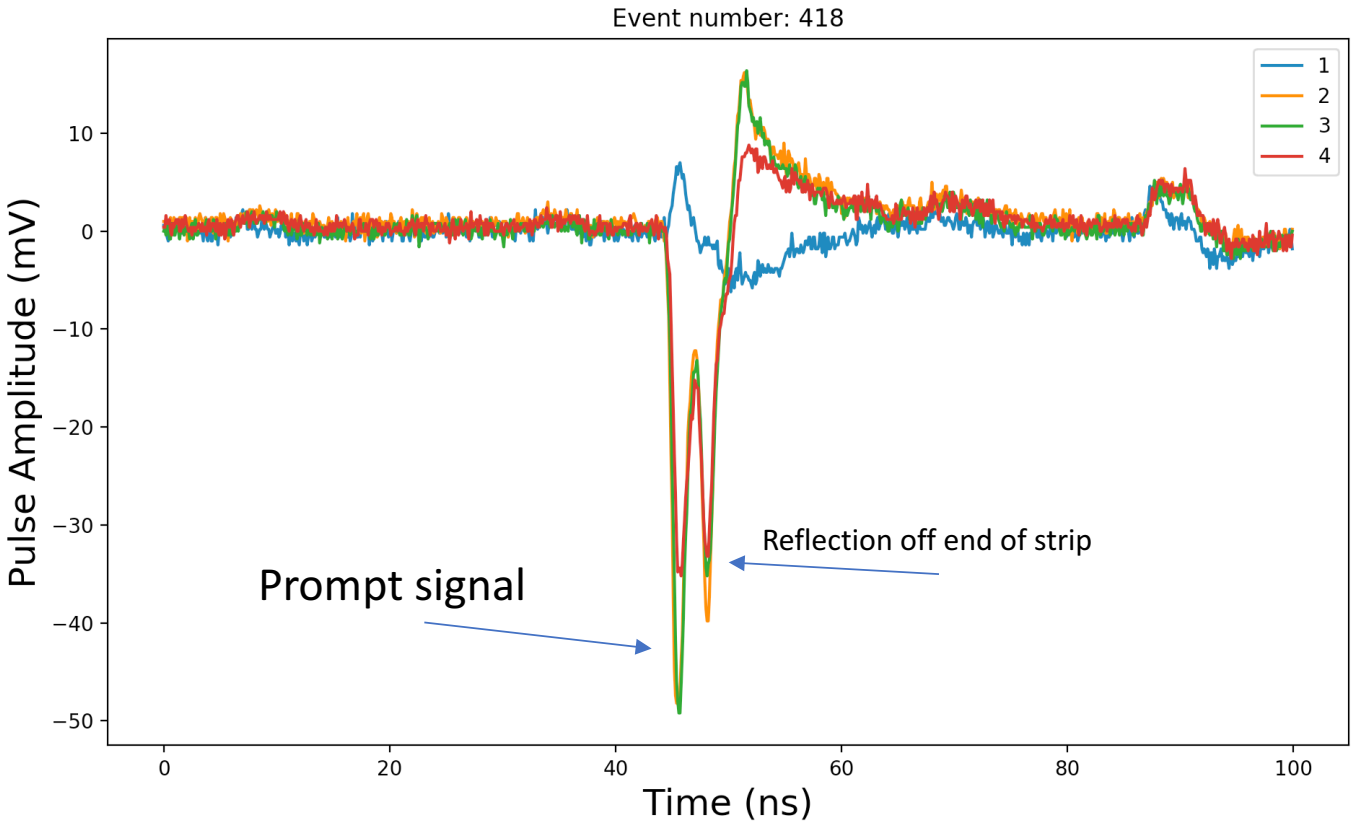


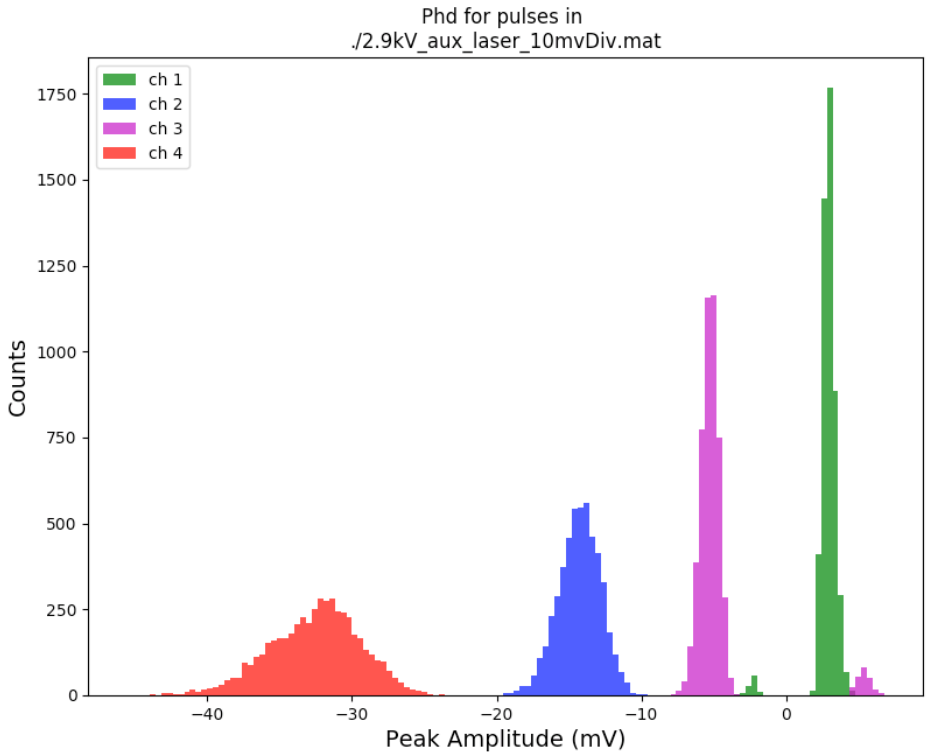
After 48 hours of cesiation

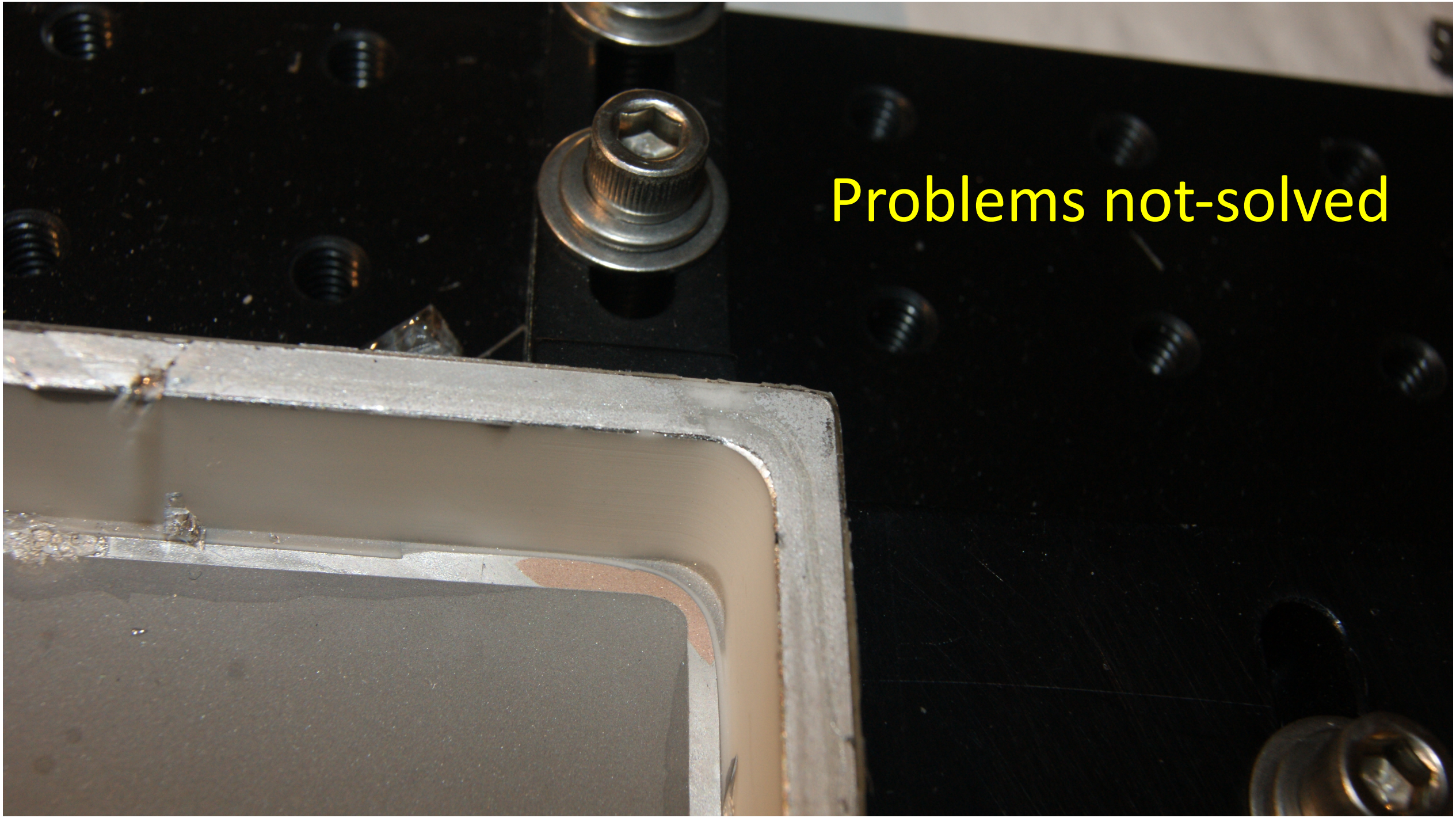


Increase j-tube from 145C-190C, cesiate for 2 hours then close source, and sit for 50 hours








Problems not-solved

Ceramic package seal – we don't have a working recipe

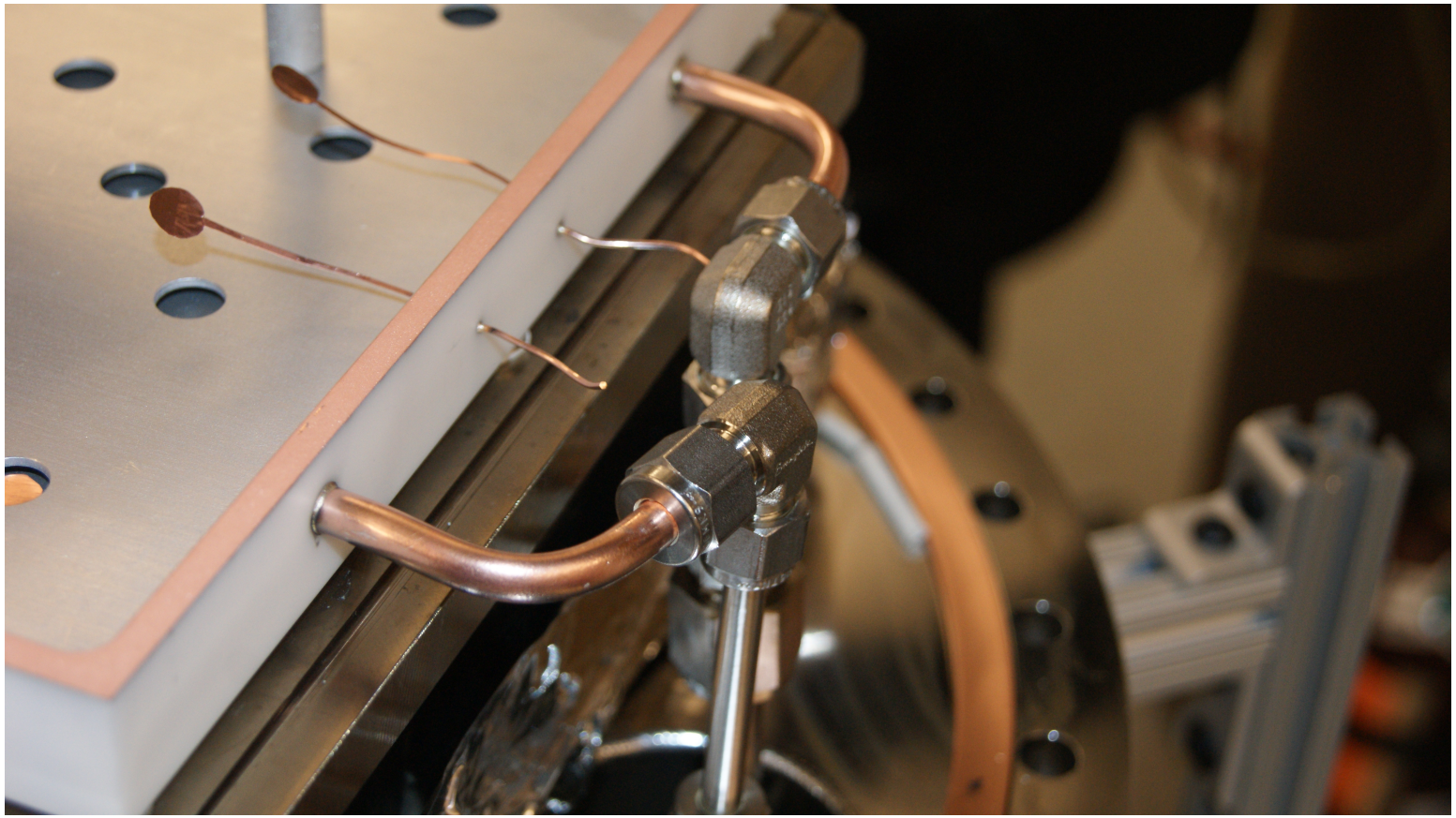
- Tile 14, 16, 17, 18, 20 leaked
- Tile 21, 22, 23, 24…
- Each vendor may have:
  - Different ceramic purity
  - Different grinding/finish/polish
  - Different heat treatment of ceramic
  - Different deposition mechanism
  - Different attention to cleanliness
  - …

Tile 24 is the most promising:
Friatec-Abrisa-B270 window

Ceramic/ Coating	Aremco	Ice	Coorstek	Friatec
Incom				
Clausing				
Abrisa				

Many combinations to try

~~Leaking brazed tubes and pin feedthroughs~~



Tile 24, brazed by Friatec has completely hermetic pins and tubes after heat cycle!

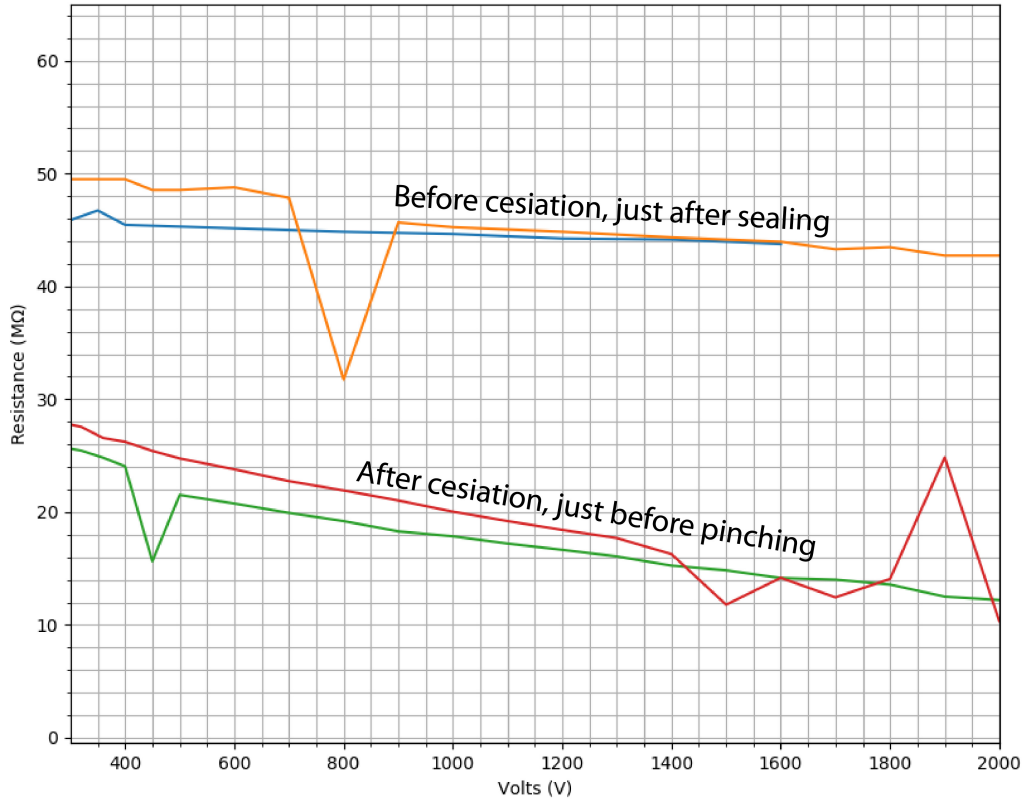
Only one trial though…

Photocathode: (subject of session 5)

We do not have a proven process to form a Cs-Sb photocathode with QE > 5%

Most recent procedure:

1. Open Cs valve, source at 145C
2. At 50 h, increase the source temperature to 185C
3. Close 2 hours after reaching hotter temperature



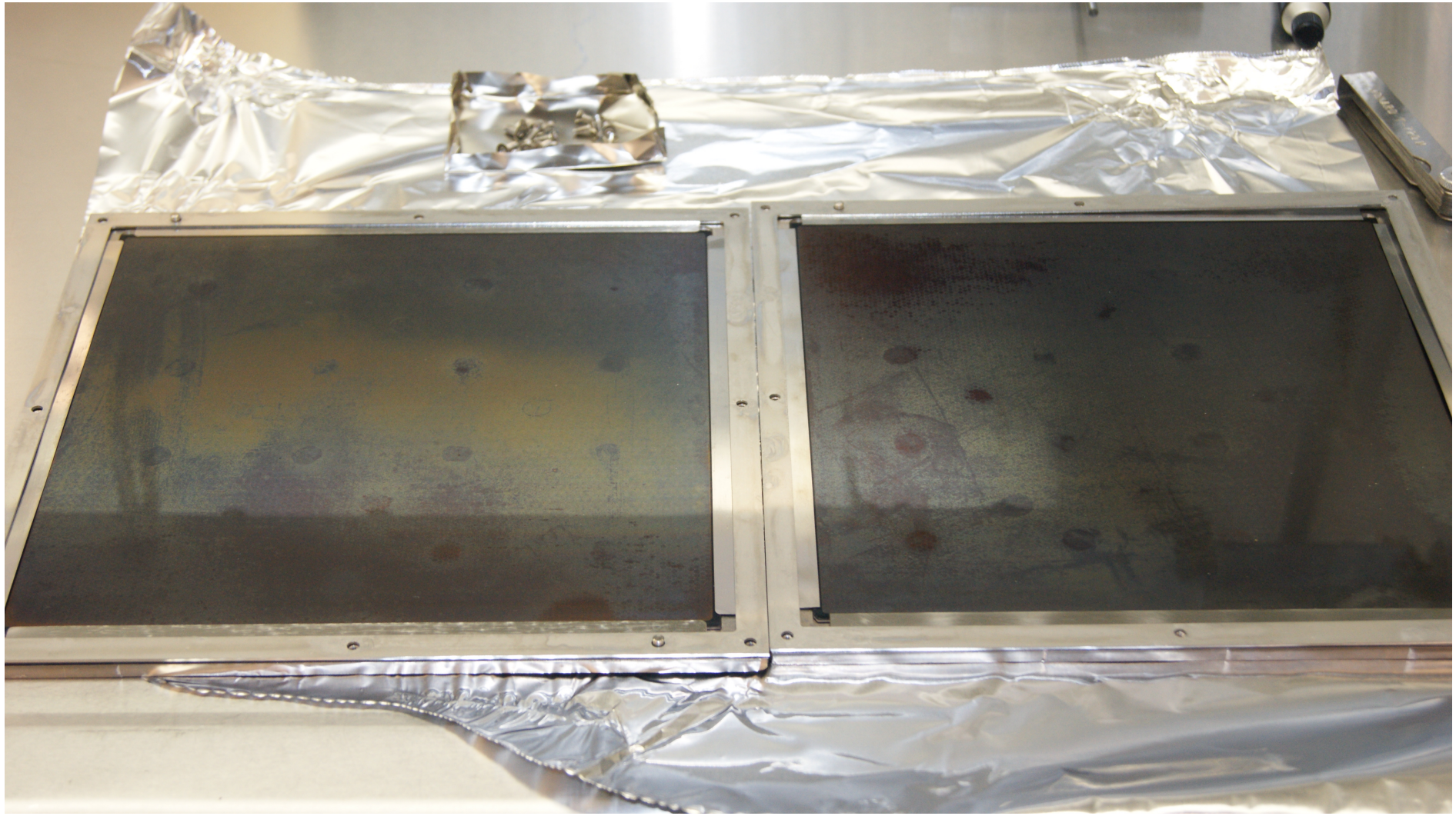
Result:

- Photosensitivity everywhere (not uniform, >30%?)
- Reduction in total stack resistance
- BUT, MCPs survive enough to produce high gain pulses on 30 strip-line capacitive readout

Need a QE measurement, no QE measurement thus far → **External voltage divider**

MCP production bottle-neck

- Reusing MCPs
- Arradiance



In summary: after various improvements…

- We do not have a proven ceramic package seal recipe
- We do not have a proven process for forming Cs-Sb photocathode with QE > 5%
- There is an MCP production bottle-neck