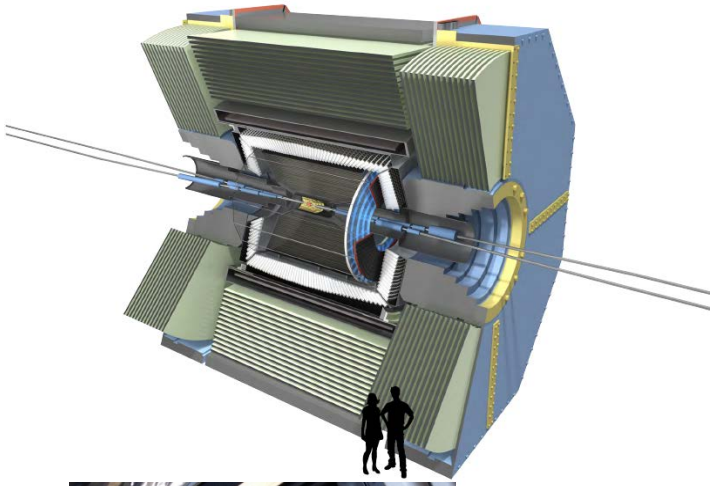
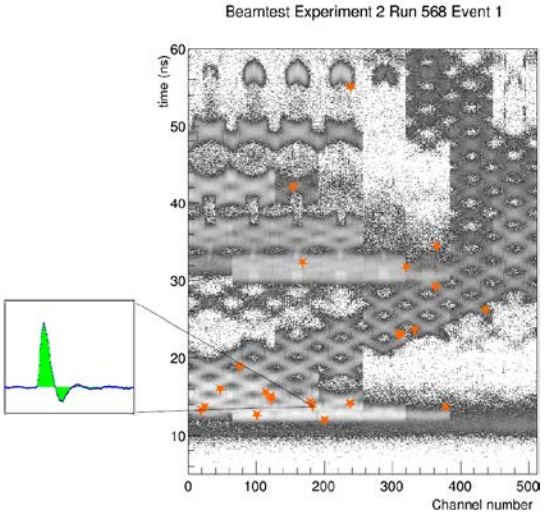
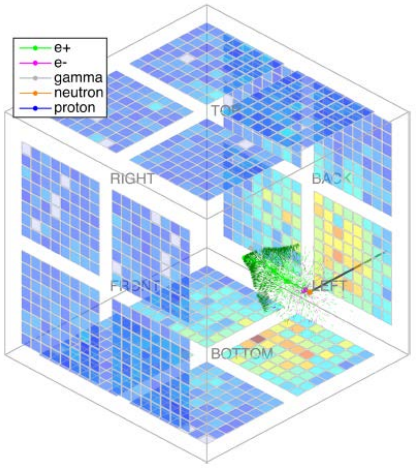
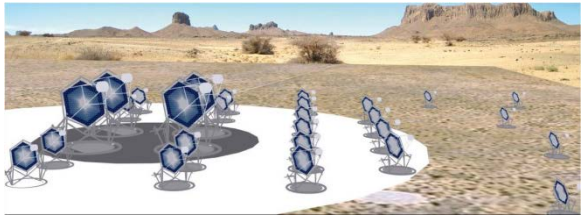
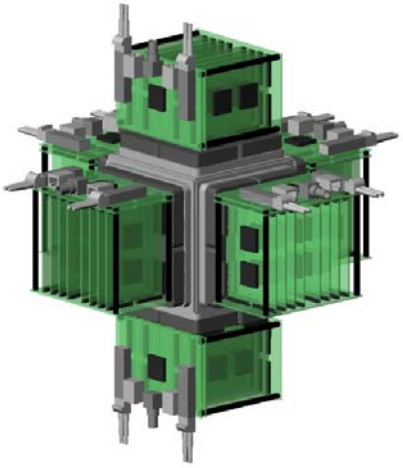
Some alternatives for Liquid Scintillator Readout









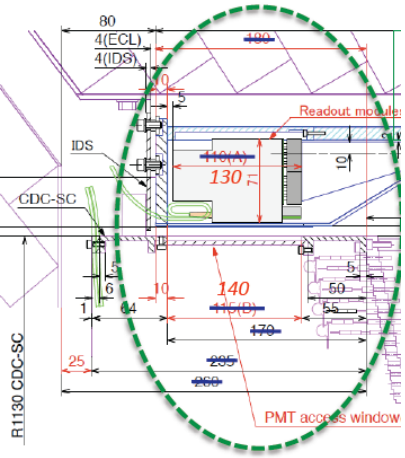


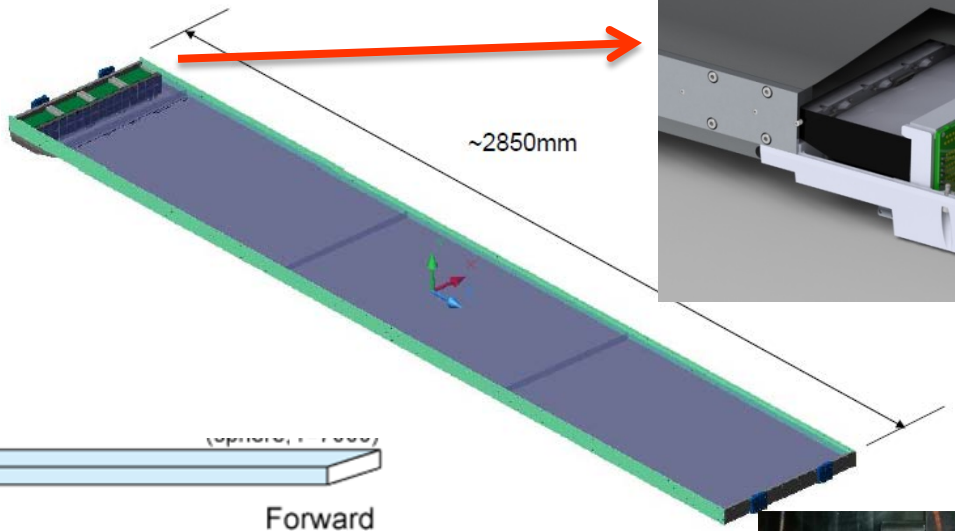
Gary Varner

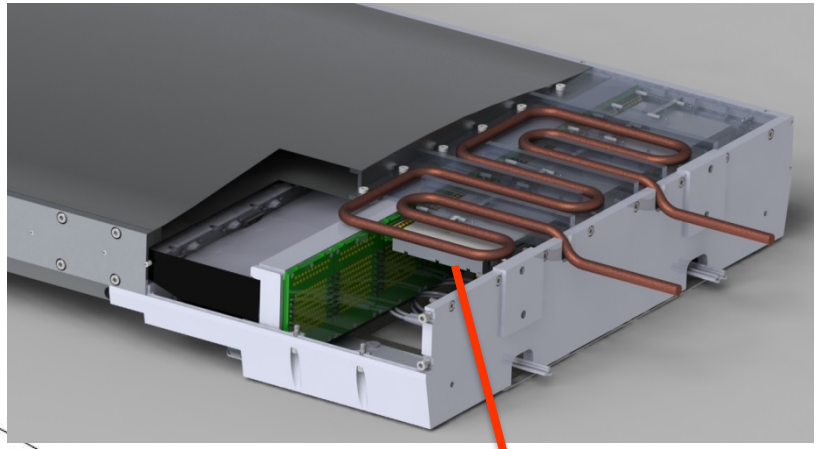
UNIVERSITY of HAWAI'I® MĀNOA

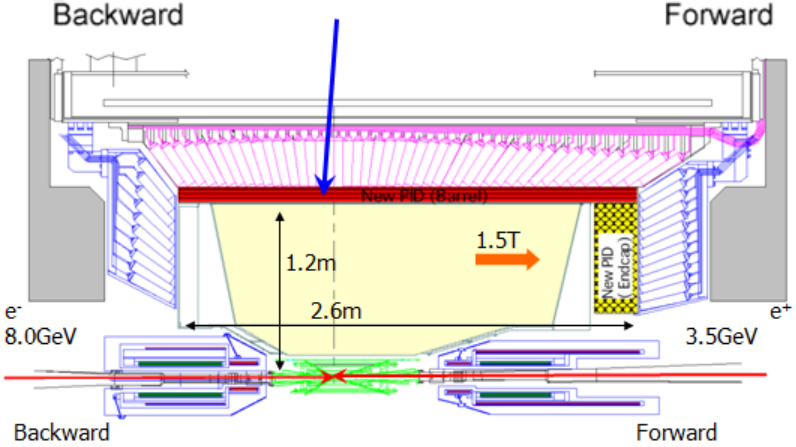
An example of highly integrated readout

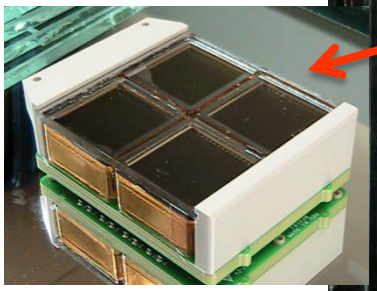
- A highly constrained space

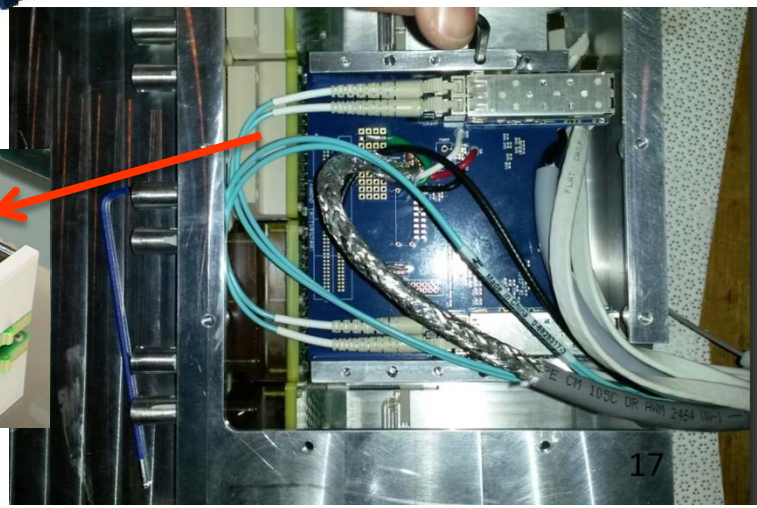








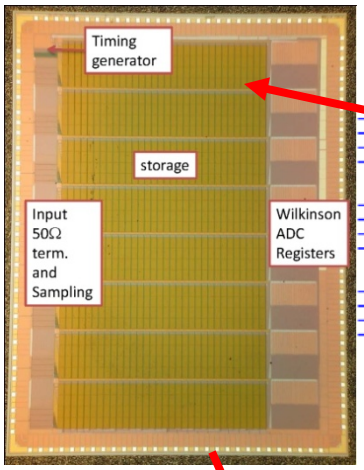


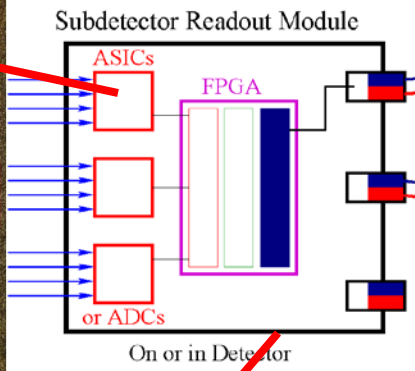


iTOP Readout

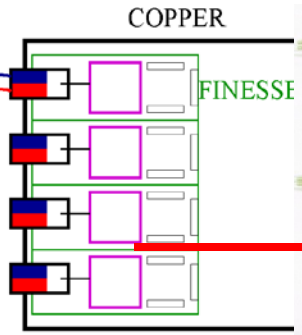
Waveform sampling ASIC

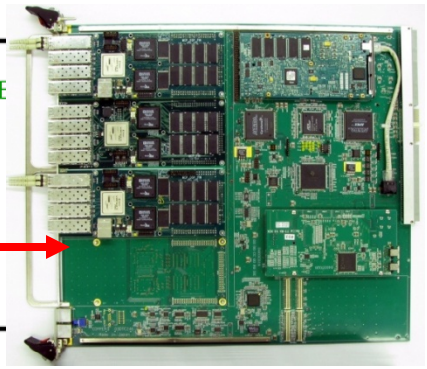
64 DAQ fiber transceivers



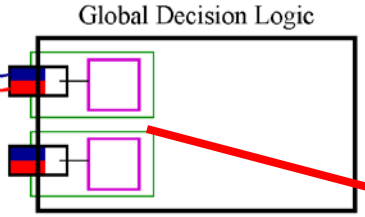


Giga-bit Fiber Transceiver Links





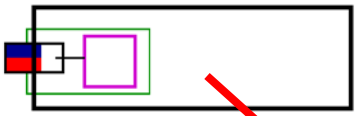
64 FINESSE
16 COPPER



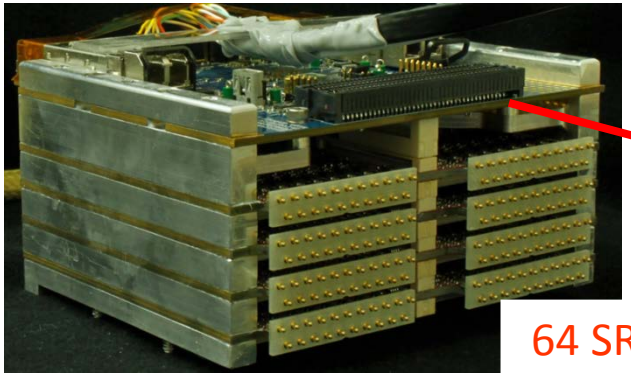
2x UT3 Trigger modules

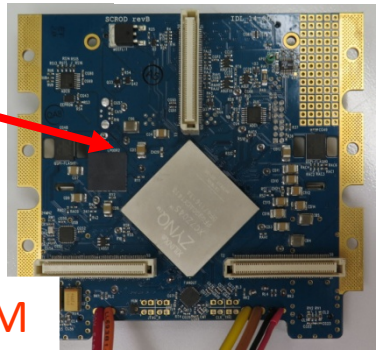
FPGA firmware consists of 3 parts:
1) ASIC/ADC driver (common)
2) Trigger/feature extract (subdet. specific)
3) Unified DAQ transport protocol

8k channels
1k 8-ch. ASICs
64 "board stacks"



Low-jitter clock



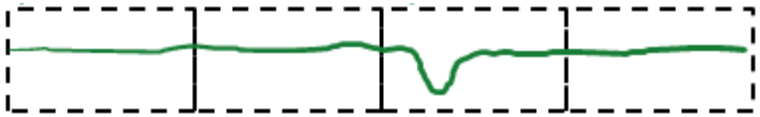


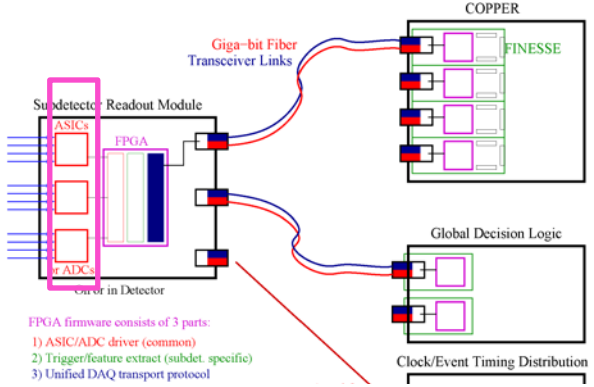
64 SRM

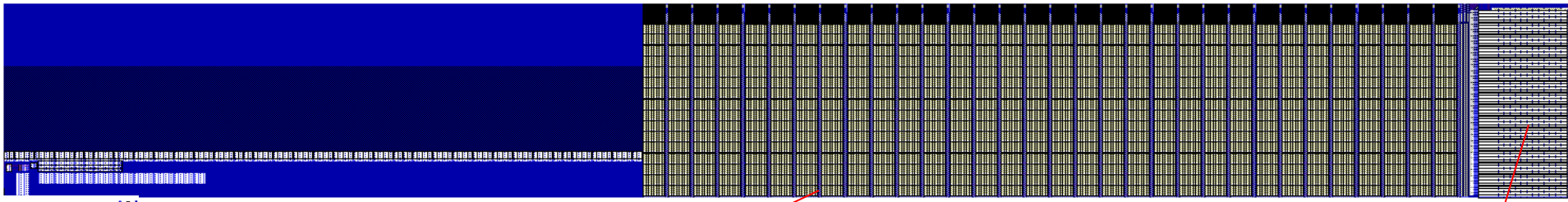
Clock, trigger, programming module (FTSW)

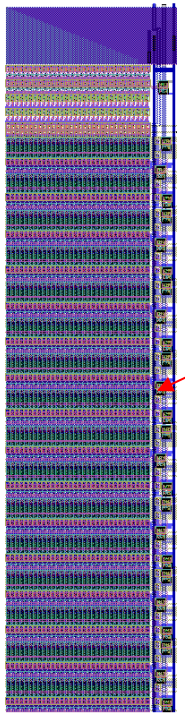
8 FTSW

Event sampling







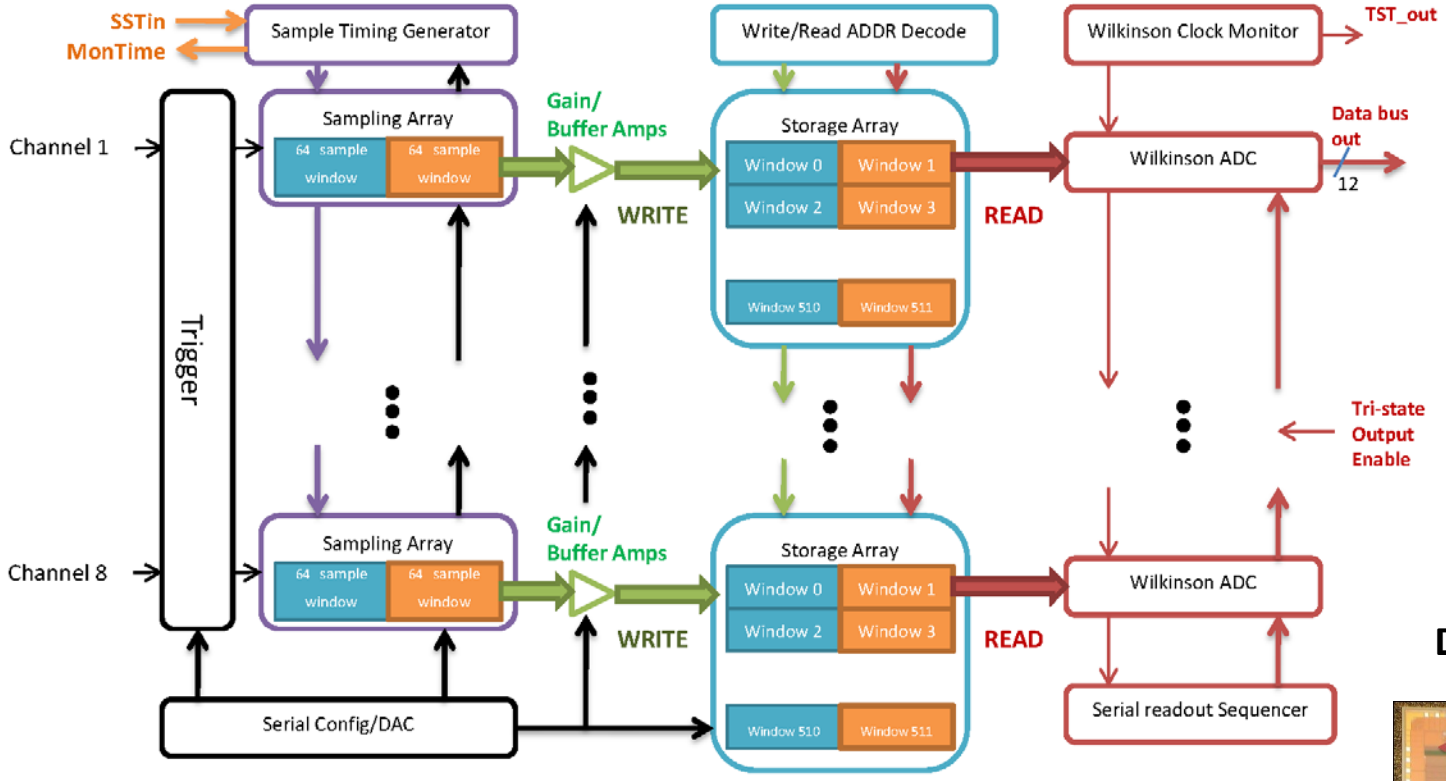


- Sampling: 128 (2x 64) separate transfer lanes

Recording in one set 64, transferring other ("ping-pong")

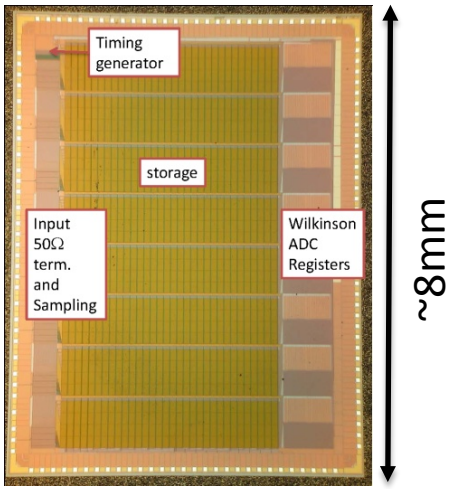
- Storage: 64 x 512 (32k per ch.)
  - Wilkinson ADC (64 at once)
  - 64 conv/channel (512 in parallel)

IRSX ASIC Overview

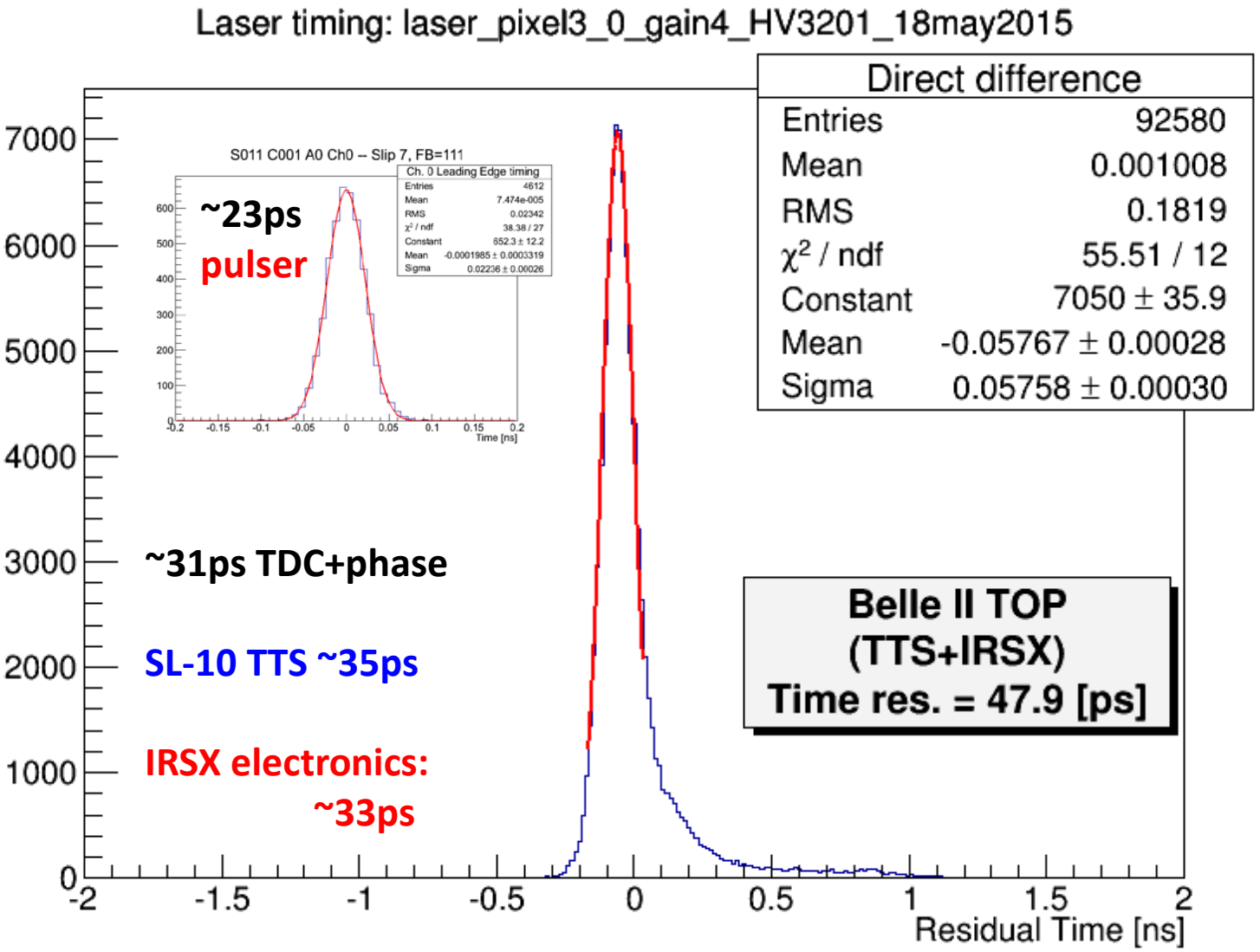


- **8 channels per chip @ 2.8 GSa/s**
- **Samples stored, 12-bit digitized in groups of 64**
- **32k samples per channel (11.6us at 2.8GSa/s)**
- **Compact ASICs implementation:**
  - **Trigger comparator and thresholding on chip**
  - **On chip ADC**
  - **Multi-hit buffering**

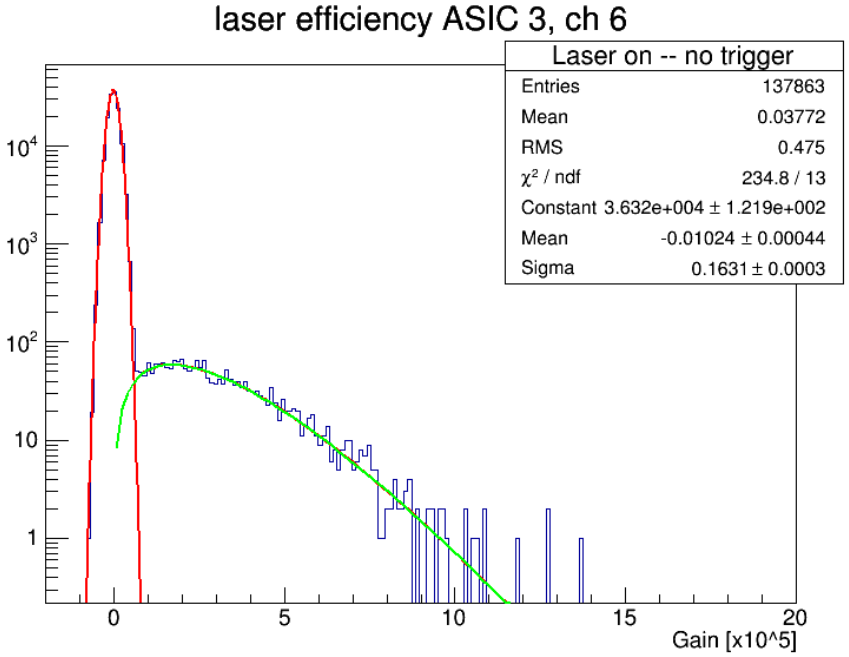
Die Photograph

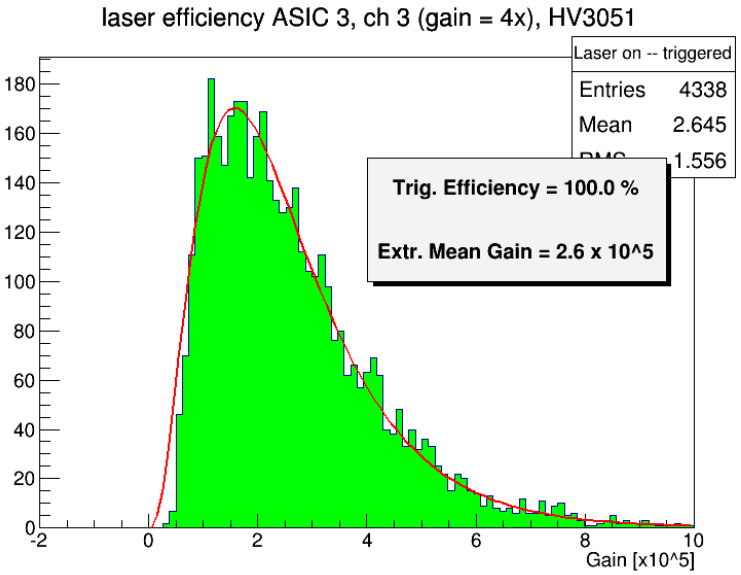


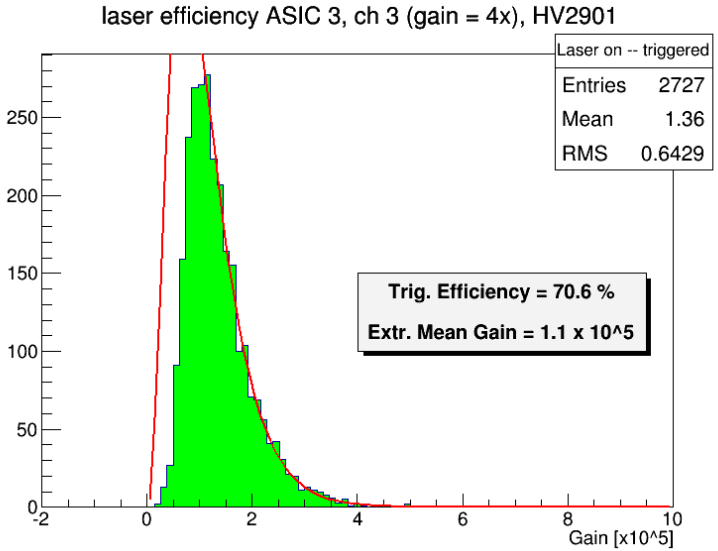
Single photon timing, 3×10^5 gain

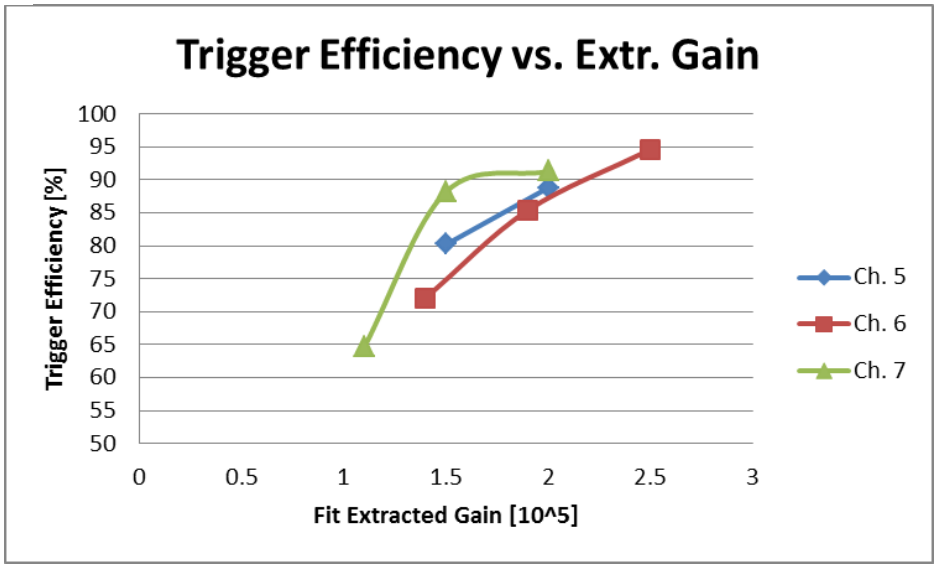


Gain and Efficiency





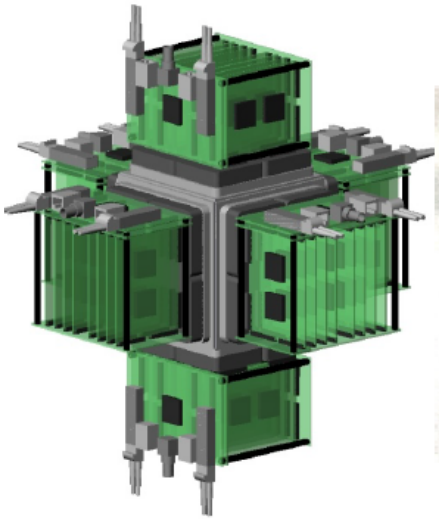


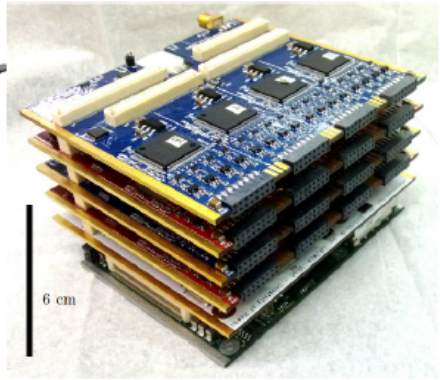


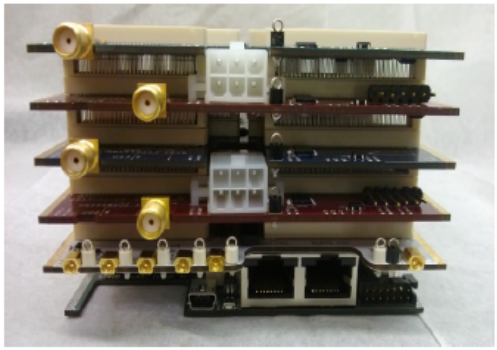
1,536 readout channels

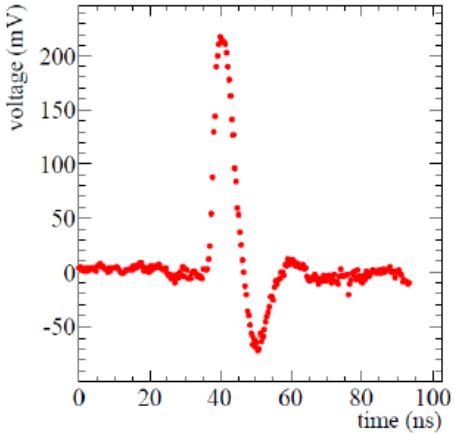
Mini Time Cube

10cm^3 detector



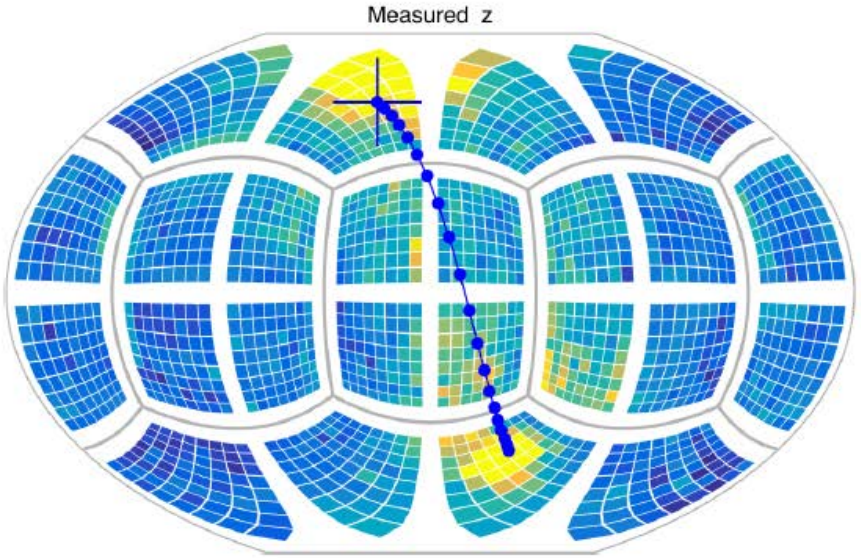






GigE readout, backend is simply PC

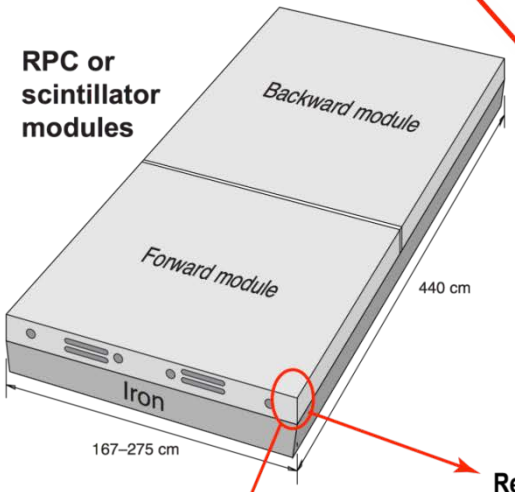
- IRS ASIC serves 8 channels.
- 4 x ASICs per “carrier board” (32 channels).
- 4 x carrier boards per “boardstack” (128 channels).
- One control board w/ FPGA per boardstack.
- One boardstack serves 2 Planacon MCP-PMTs.
- 12 boardstacks required to instrument 24 Planacons.
- Total envelope per boardstack ~10 cm x 10 cm x 8 cm.

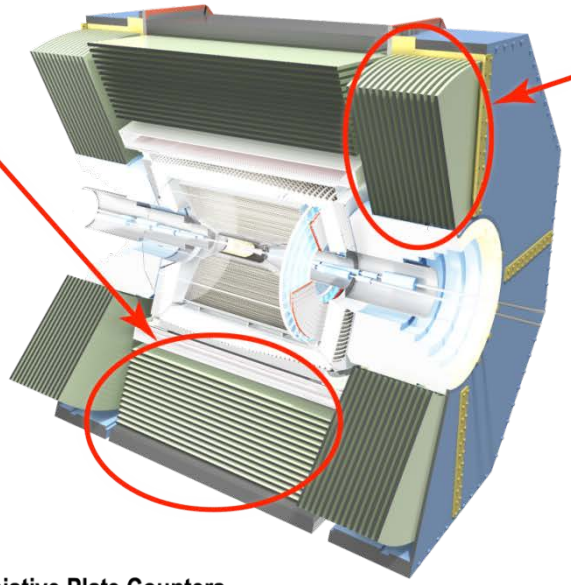


KLM Detector upgrade

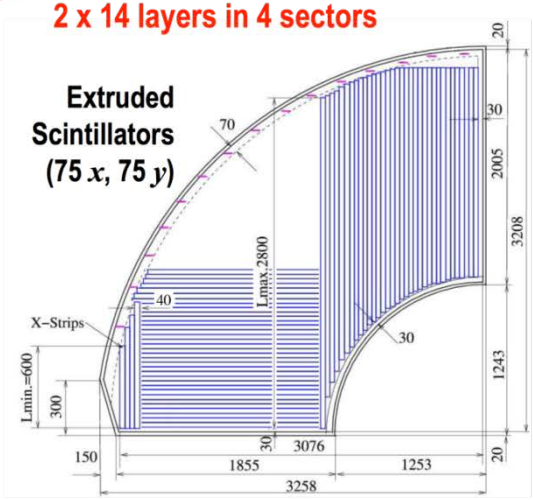
Outside the magnet, the KLM detects K_L mesons and muons

BARREL
15 layers in 8 sectors

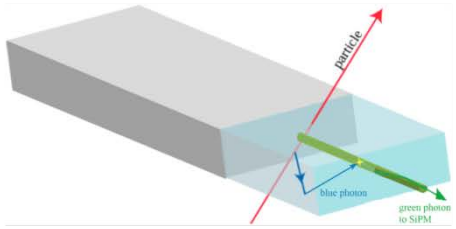




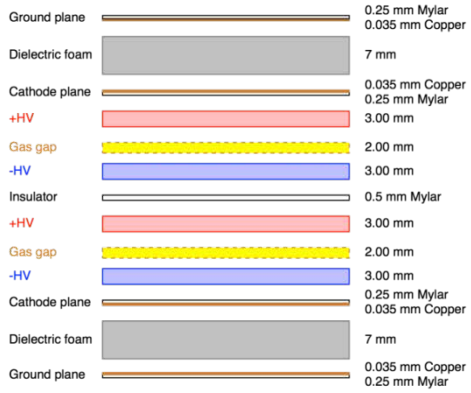
ENDCAPS (2)
2 x 14 layers in 4 sectors



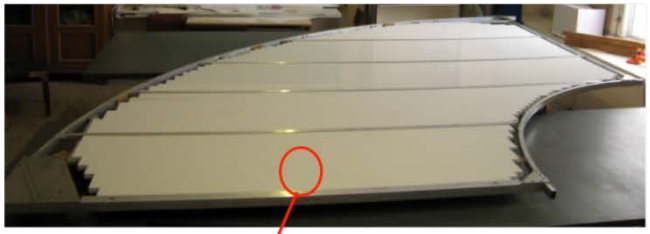
Extruded Scintillators (2 innermost layers)

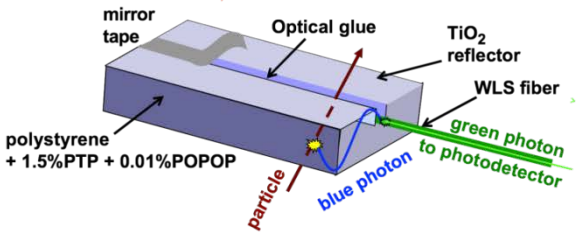


Resistive Plate Counters (13 outer layers)



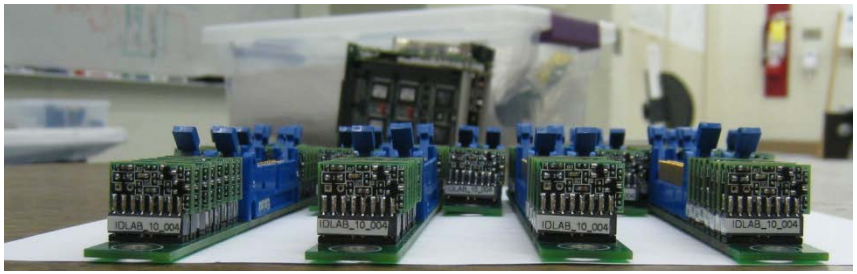
RPC cross section

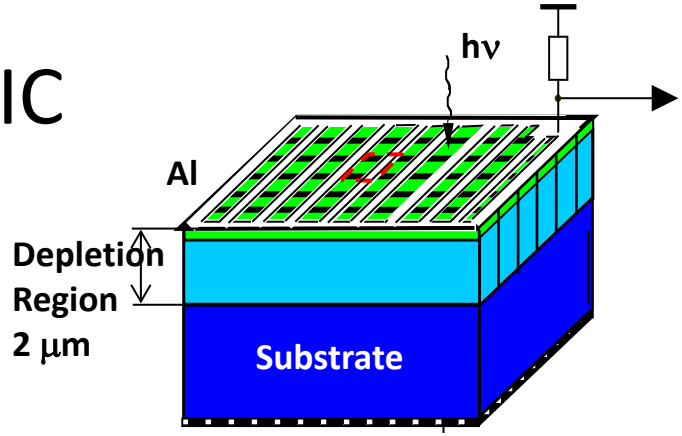


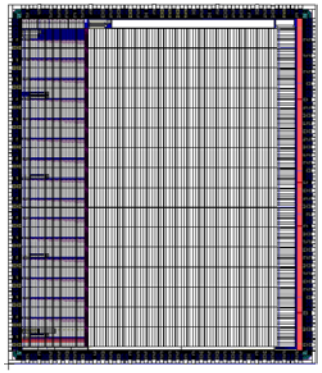


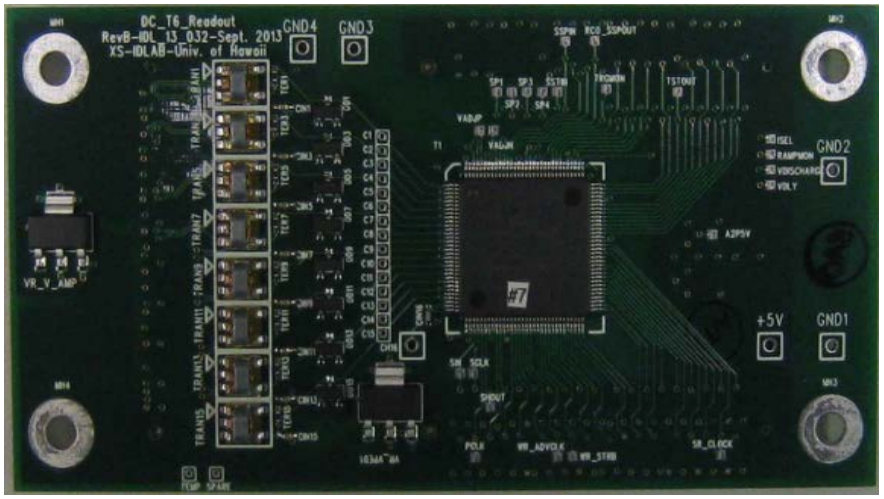
Technical Implementation

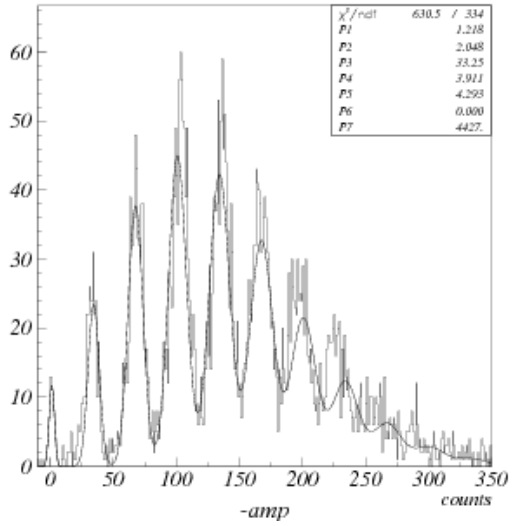
- Pre-amps and TARGET ASIC







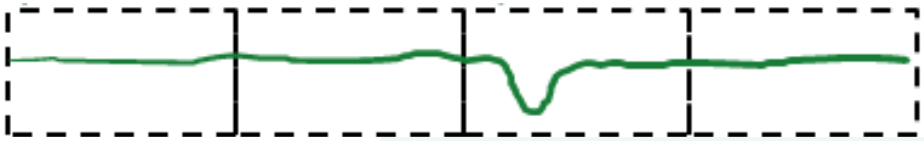


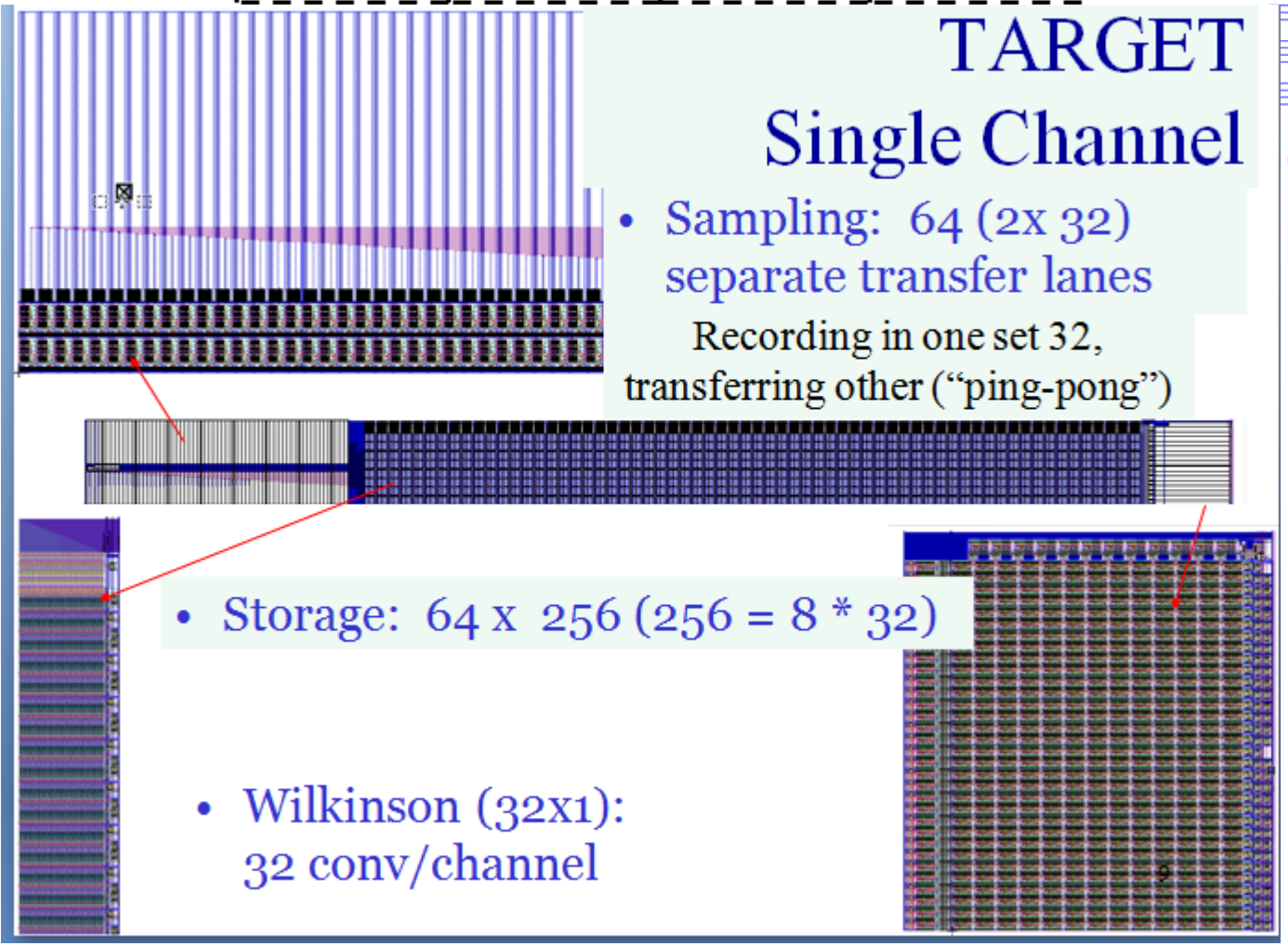


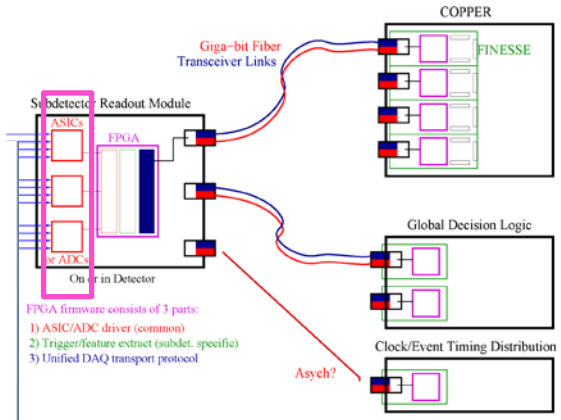
- **16 channels**
- **0.5-1.2 GSa/s**
- **10-12-bit digitization**
- **Samples stored, digitized in groups of 32**
- **16k samples per channel (16us at 1GSa/s)**
- **Integrated triggering capability**

500kHz – 2MHz dark rate not a problem:
5 p.e. threshold reduces rate to < 1kHz
while maintaining > 99% MIP efficiency

TARGET ASIC Overview







Very similar to IRSx:

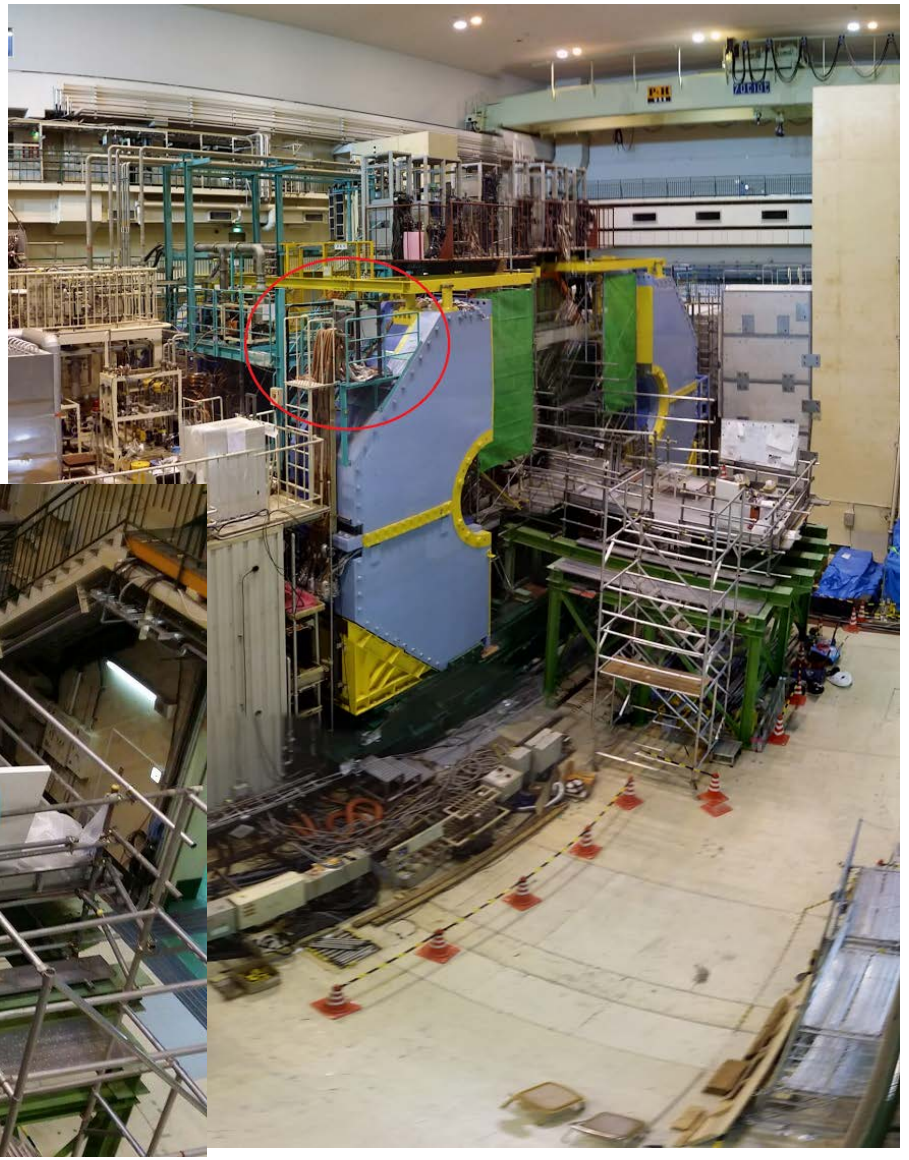
- Sampling aligned to SuperKEKB RF clock
- 2x more channels
- Sampling 3x slower
- No precision timing requirement

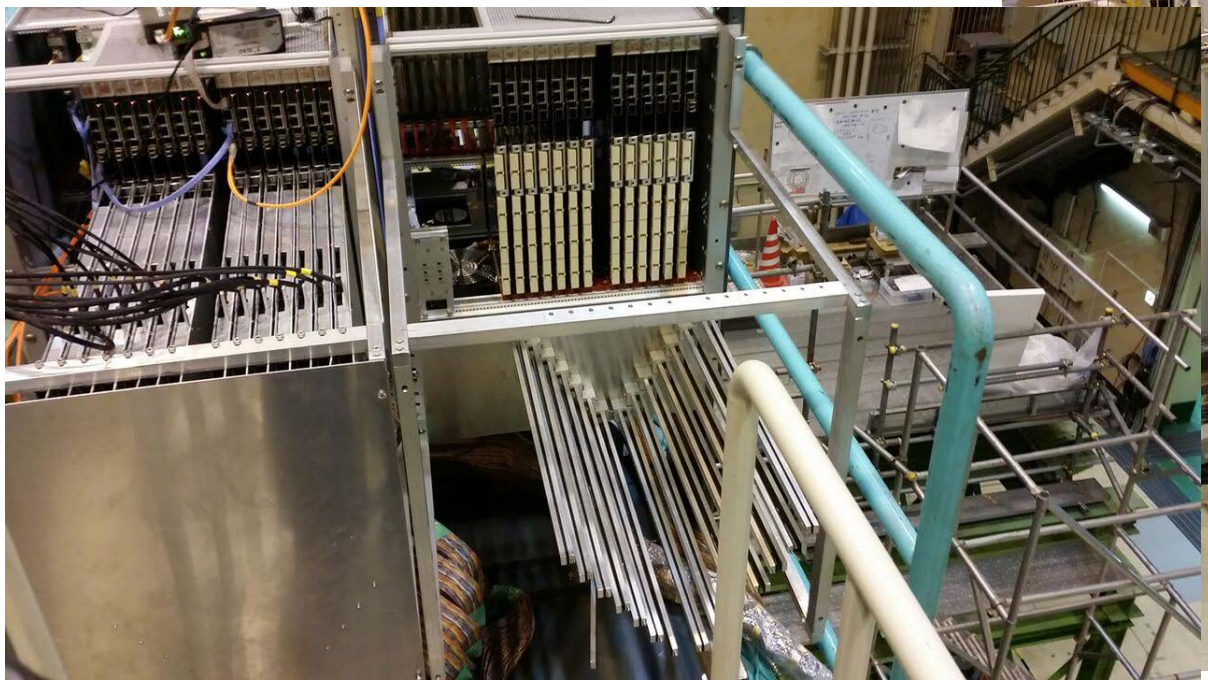
Installing at Belle II (Dec. 9, 2015)

>21,000 channels fabricated, production tested

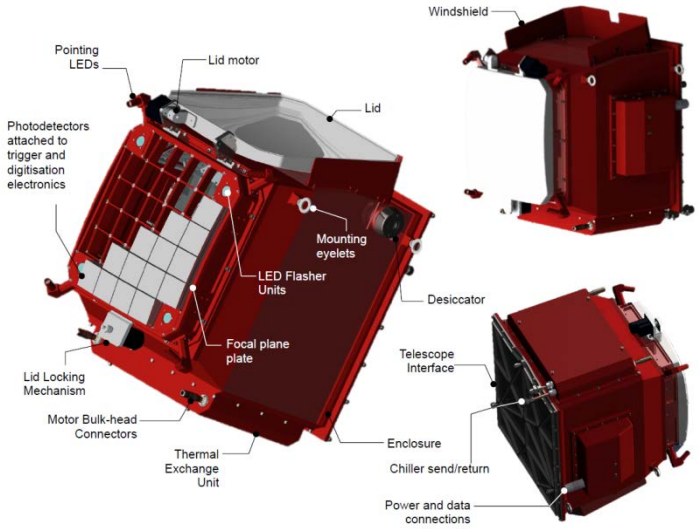
First crate installation at left:
14 9U cards of 150 channels each
(2,100 channels)

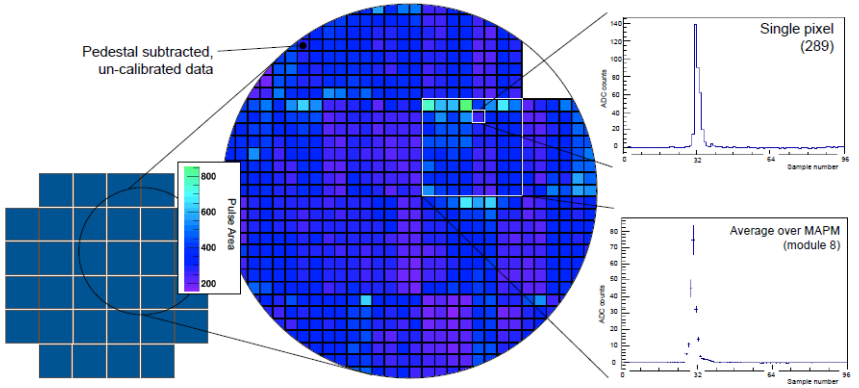
TARGETX production costs
($1.4/channel, >95% yield, incl. trigger and ADC)

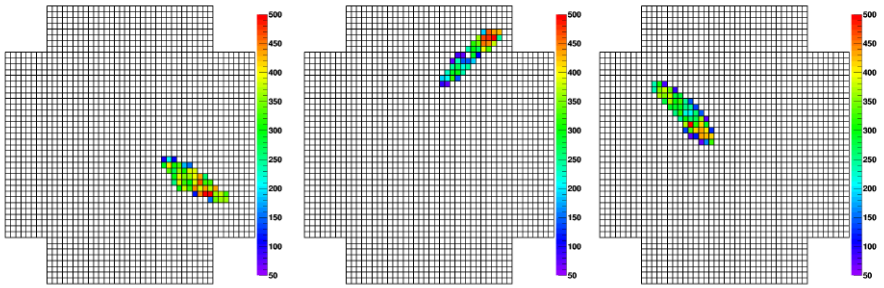


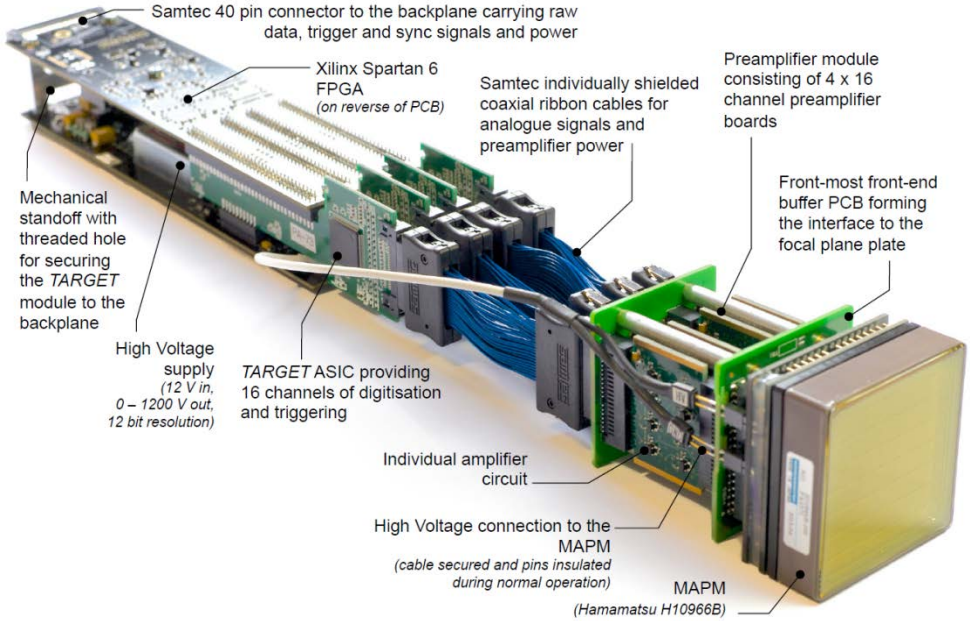


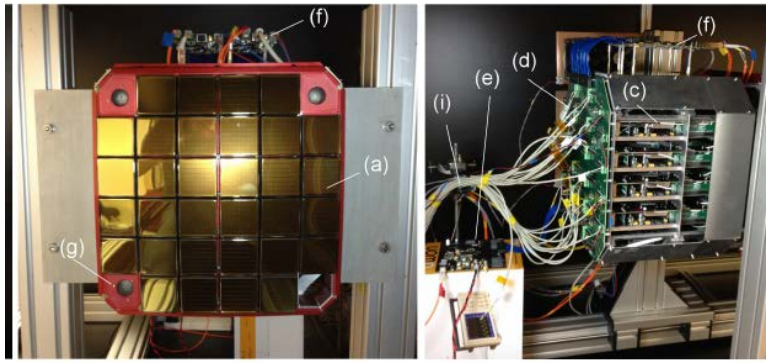
GCT Camera (CTA)



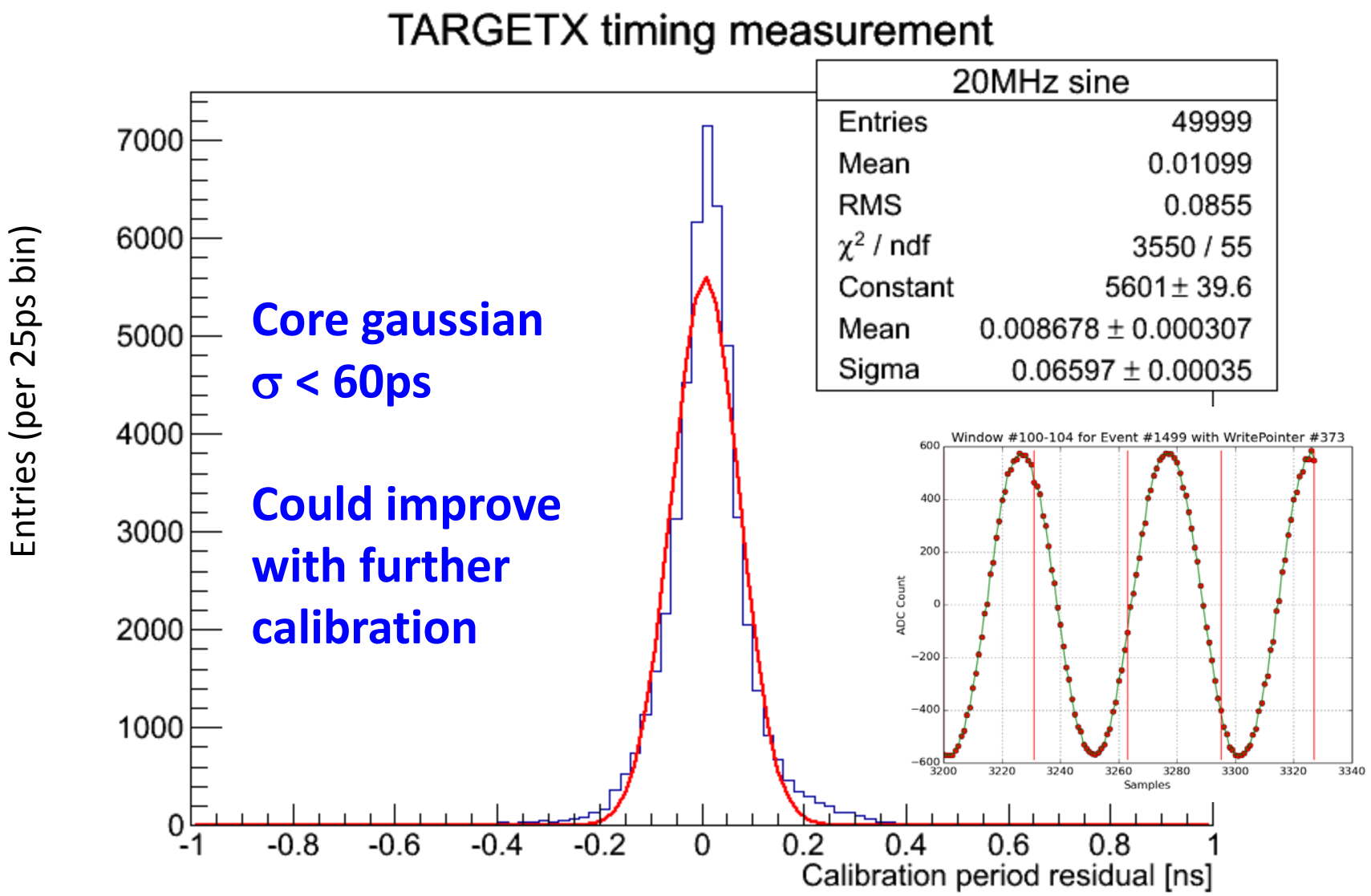








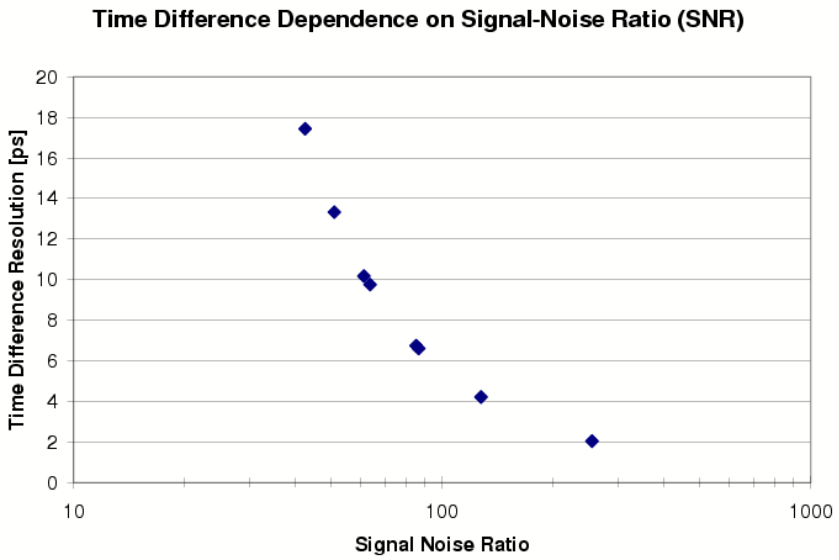
Even though not designed for precise timing…



Of course, still pushing envelope on timing

- Noise/amplitude
- Non-linearity
- Timebase non-uniformity

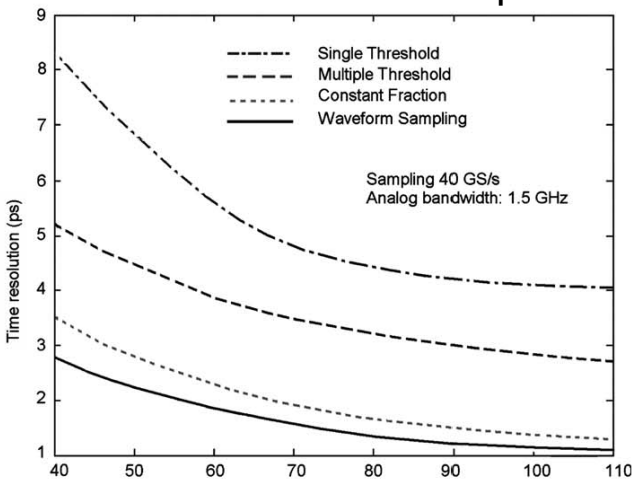
1GHz analog bandwidth, 5GSa/s



G. Varner and L. Ruckman

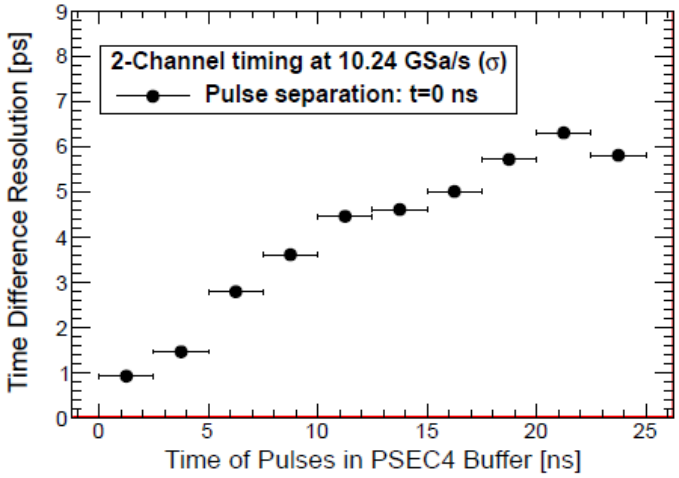
NIM A**602 (2009) 438-445**.

Simulation includes MCP response

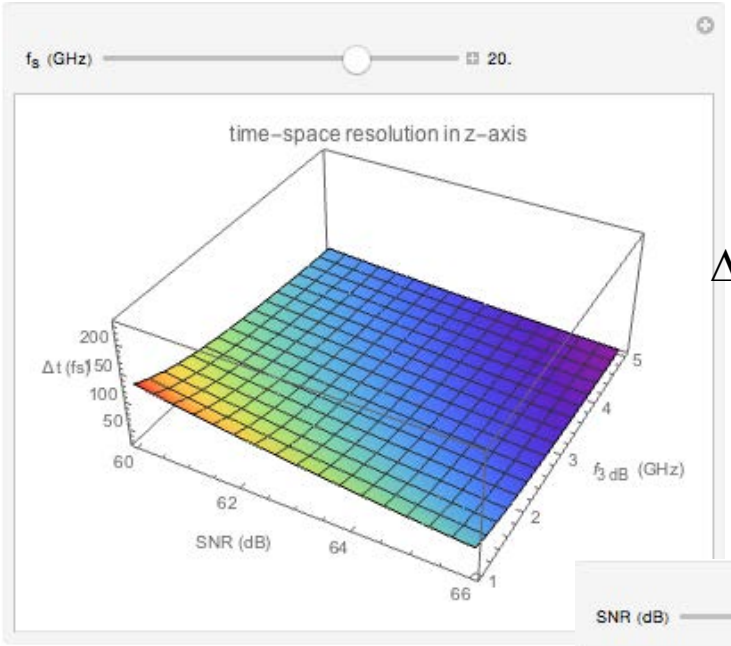


J-F Genat, G. Varner, F. Tang, H. Frisch

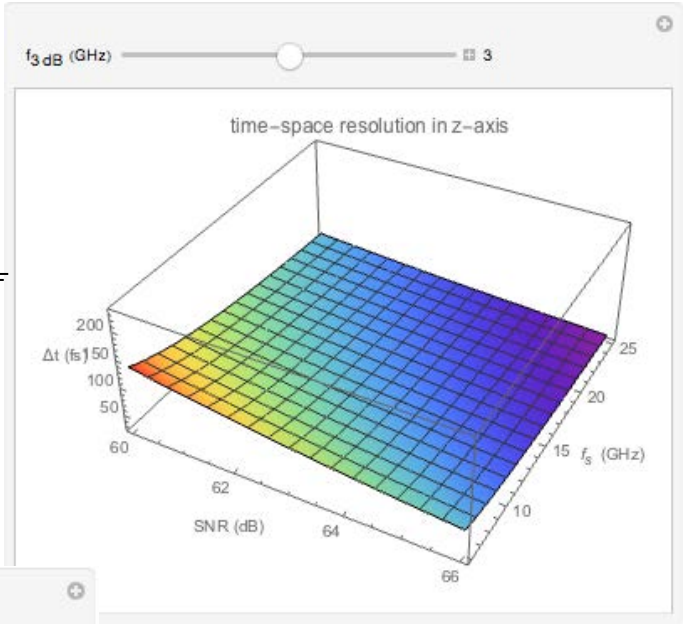
NIM A**607 (2009) 387-393**.

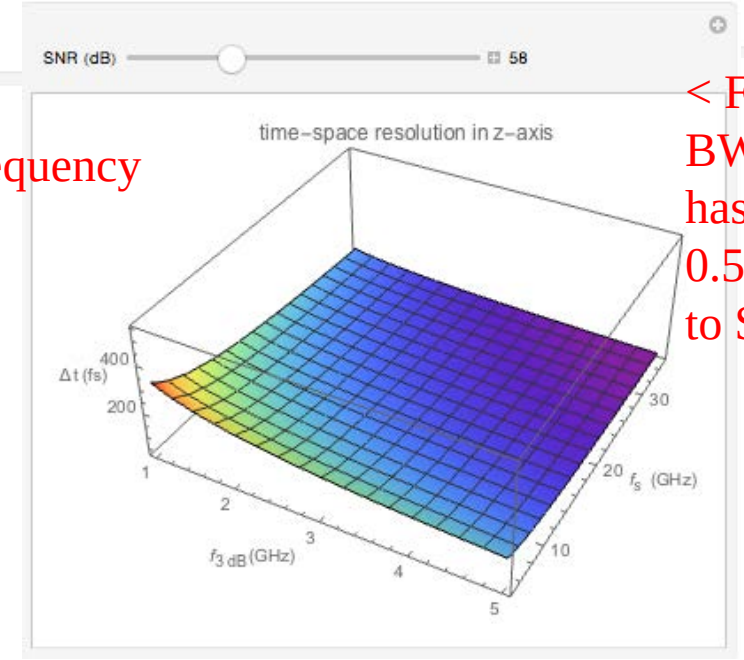


A detailed study of Z-by-t (Si tracker Orel PhD)



$$\Delta t = \frac{\Delta U}{U}\frac{1}{\sqrt{0.34 * BW * f_s}}$$





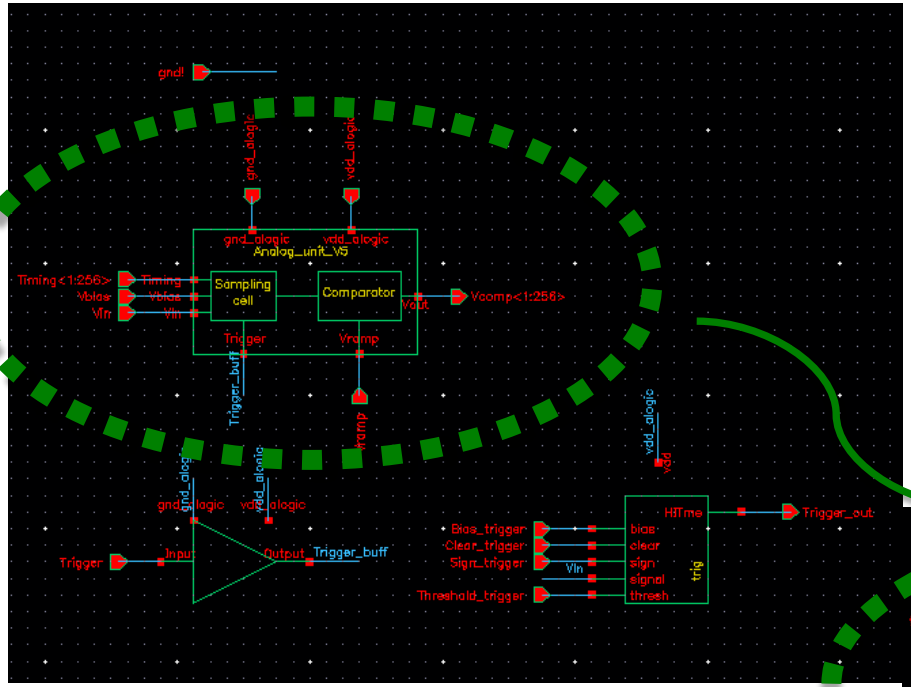
^ Need to hold sampling frequency to least at 20 GHz to have timing resolution in 100fs range

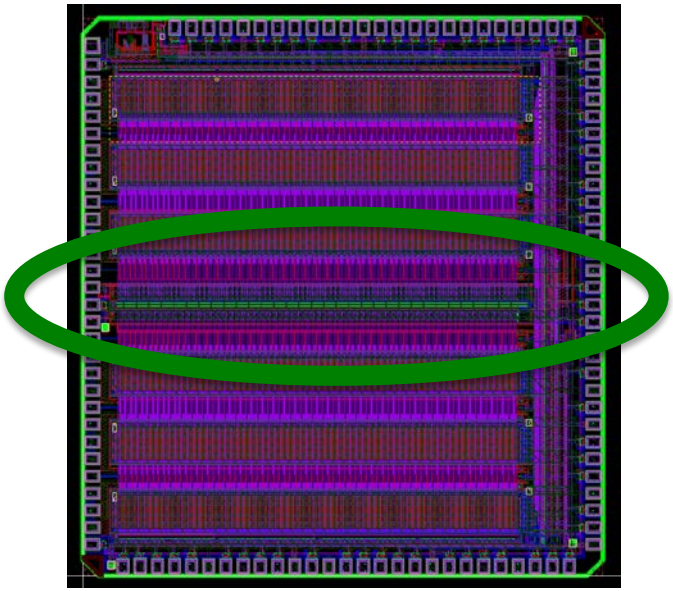
< For the above sampling freq and BW integrated noise amplitude has to be in the range or less than 0.5mV to 0.6mV corresponding to SNR~58dB (V_{pp}=1volts)

SNR~58dB corresponds to 9.4 bits for 20μm resolution in rφ (Ideal ADC)

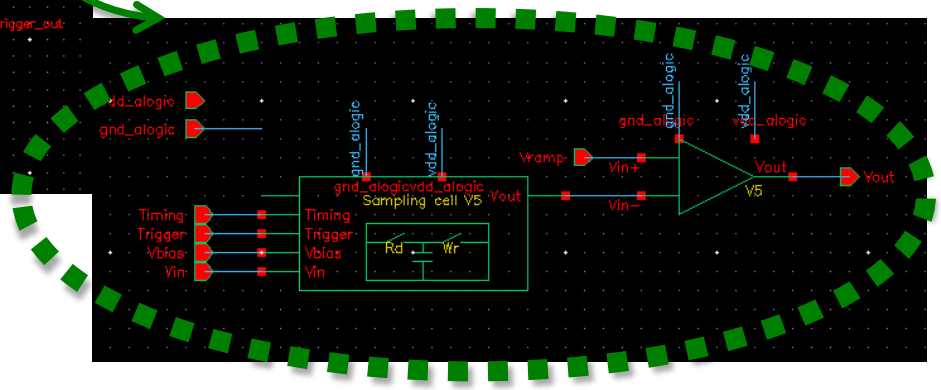
PSEC4: Sampling Analysis

Utilizing PSEC4's SCA as starting place
-Adjustable Sampling rate between 4-15 GSPS
-1.6 GHz bandwidth





x256



also
-0.13µm CMOS (IBM-8RF)
-10.5 bit DC dynamics

Summary – Requirements comparison

Parameter	Measured (worst cases)	Requirement
Bandwidth (Single cell)	1.7GHz @665Vdc @50Ω	3GHz
Bandwidth (Multi cell)	1.0GHz @665Vdc @50Ω	3GHz
SNR	61.7 dB	58dB
ENOB	9.8 bits (small region)	9.4 bits

Things to improve:

- **Reduce Ron variance over the dynamic range to reduce distortion and increase the ENOB**
- **Bandwidth dominated by Cin:**
  - **Reduce Cin or reshape the channel to increase the bandwidth (first pole)**
  - **Reduce Ron overall value to increase the bandwidth (second pole)**
- **Speed dominated by bandwidth:**
  - **Increase bandwidth**
  - **Overlapping of sampling cell windows to increase the effective sampling frequency**
- **Use differential configuration to reduce pedestal error and increase noise coupling and crosstalk immunity**

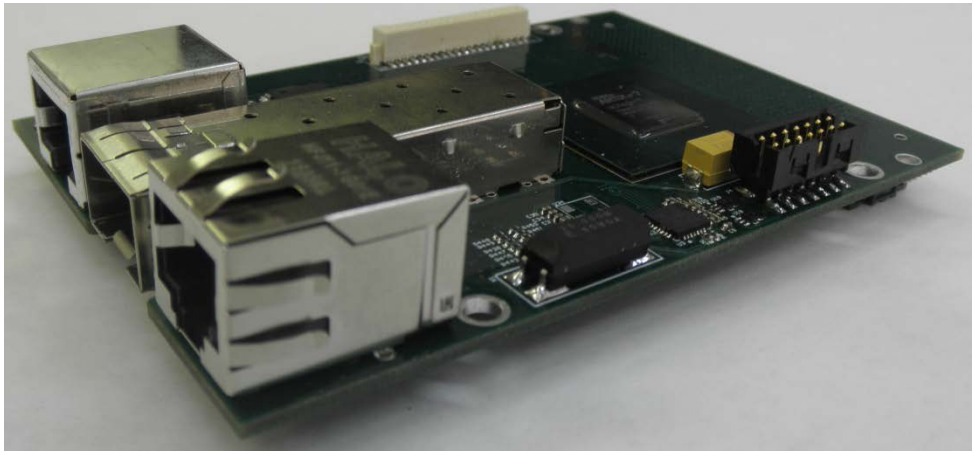
ASICs in the works

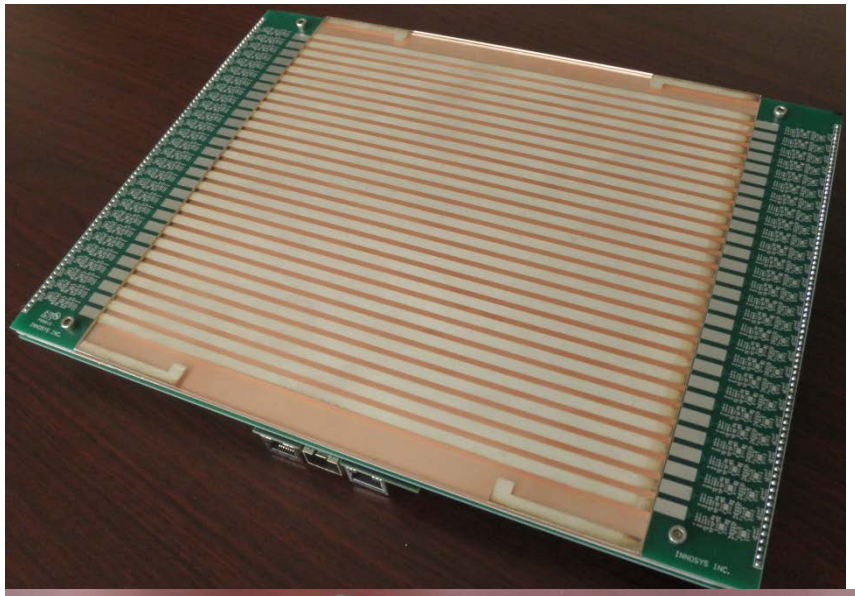
- Low-power, 64 channel ASIC (ALPS)
- PSEC5 ASIC
  - 256 → 32k sample storage
  - Work to optimize bandwidth, ENOB
  - Persistence effects
- RFpix ASIC
  - Push limits of ABW, timing
  - Below 100-200fs, direct spatial measurement becomes interesting
  - Many practical issues, but none fundamental (CF 1ps)
- DRS5, SAMPIC ASICs
  - Will be interesting to see how well can perform

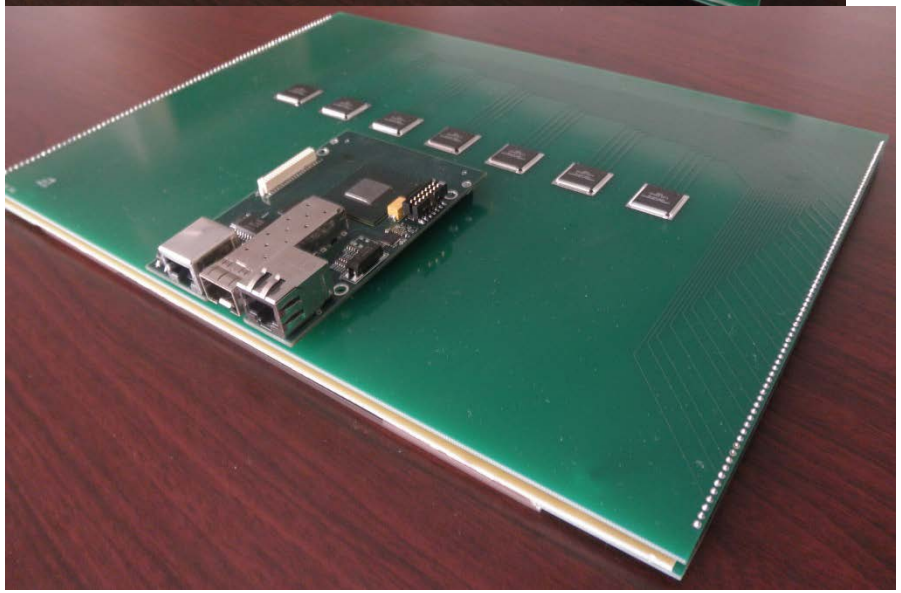
Toward increased timing precision

ASIC	# chan	Depth/chan	Time Resolution [ps]	Vendor	Size [nm]	Year
LABRADOR 3	8	260	16	TSMC	250	2005
BLAB	1	65536	1-4	TSMC	250	2009
STURM2	8	4x8	<10 (3GHz ABW)	TSMC	250	2010
DRS4	8	1024	~1 (short baseline)	IBM	250	2014
PSEC4	6	256	~1 (short baseline)	IBM	130	2014
RITC3	3	Continuous	TBD	IBM	130	---
PSEC5	4	32768	TBD	TSMC	130	---
DRS5	8/16?	128x32	TBD	UMC	110	---
SamPic	16	64	~3 [pic 0]	AMS	180	[2014]
RFpix	128?	TBD	<= 100fs (target)	TSMC	45 ?	---

Commercializing Control/Readout







- Scalable Triggered Readout and Advanced Processing (STRAP)
- DOE SBIR Phase I funded first prototypes at Innosys Technologies
- Applying Phase II STTR to get these systems into field
- Initial units will use available ASICs, Innosys to commercialize P5P (separate SBIR)
- Adapter (“ASIC”) board project specific (FMC connection)

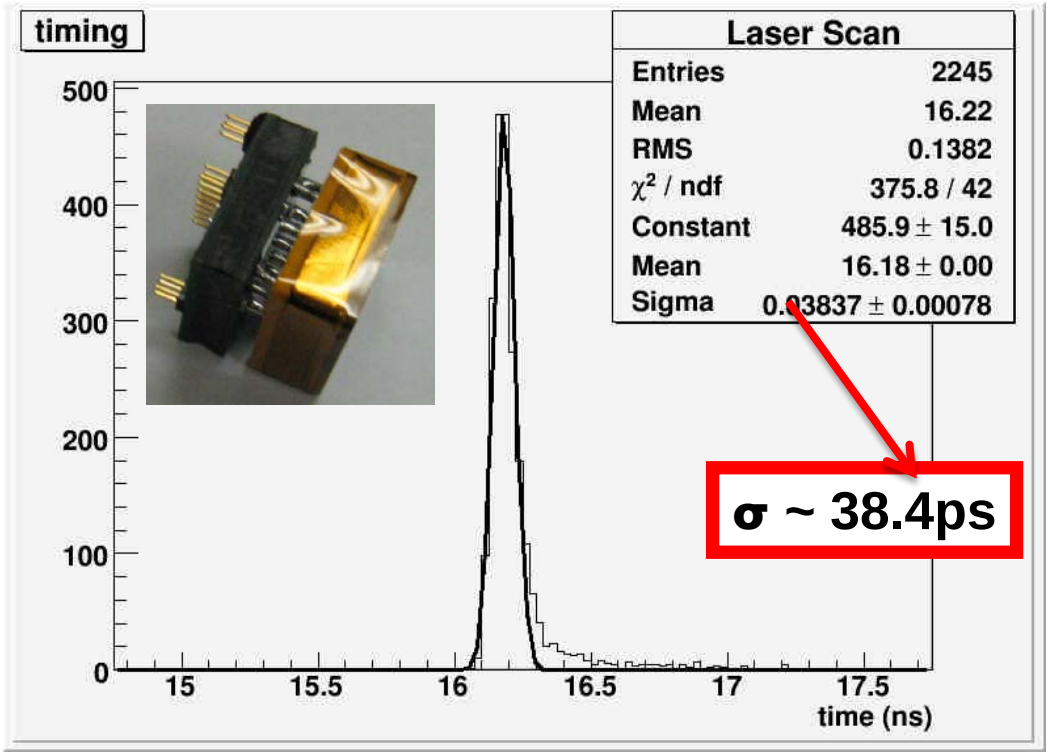
Summary of UH-centric Alternatives

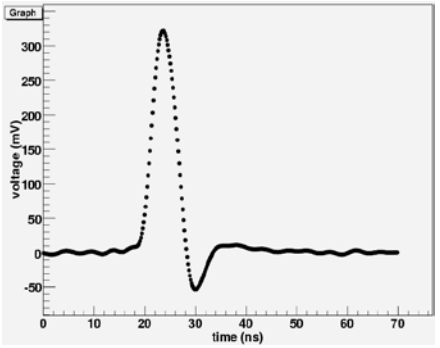
- There are now a number of alternatives that exist and additional ASICs in the pipeline
- Trade-offs on density, power, storage depth, etc.
- Having on-chip triggering and ADC functionality greatly simplifies implementation
- Moving readout state machines on-chip next
- One huge advantage of PSEC4 architecture ➔ Calibration! (or can live without doing)
- Developing a common readout infrastructure addresses the biggest headache in fielding these systems ➔ Firmware!

BACKUP

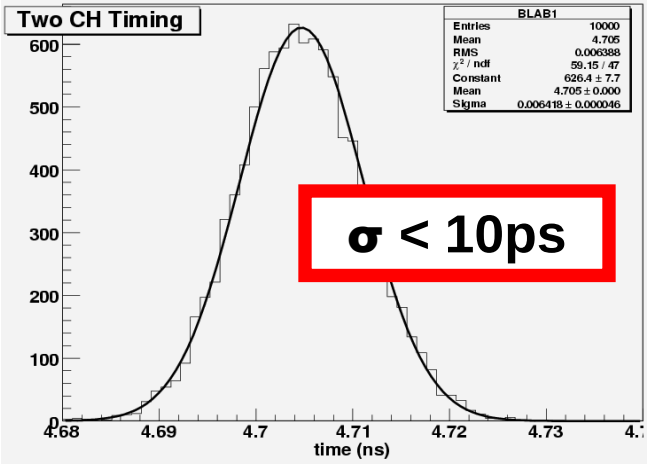
Single photon timing

- Record single photon timing with resolution comparable to MCP-PMT + System timing



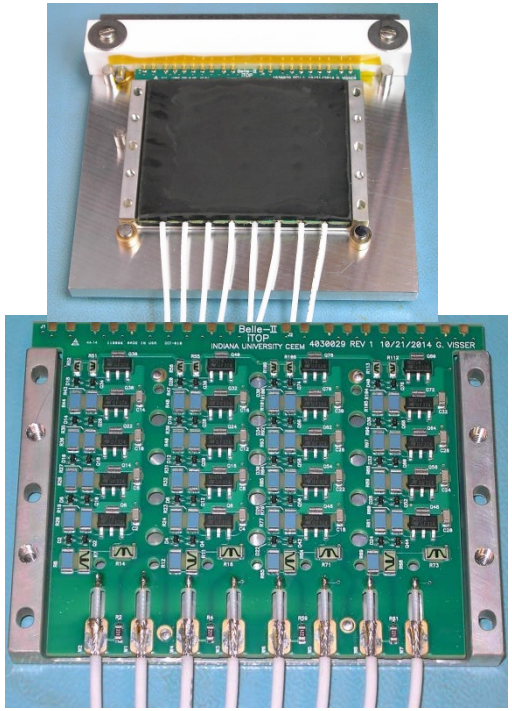


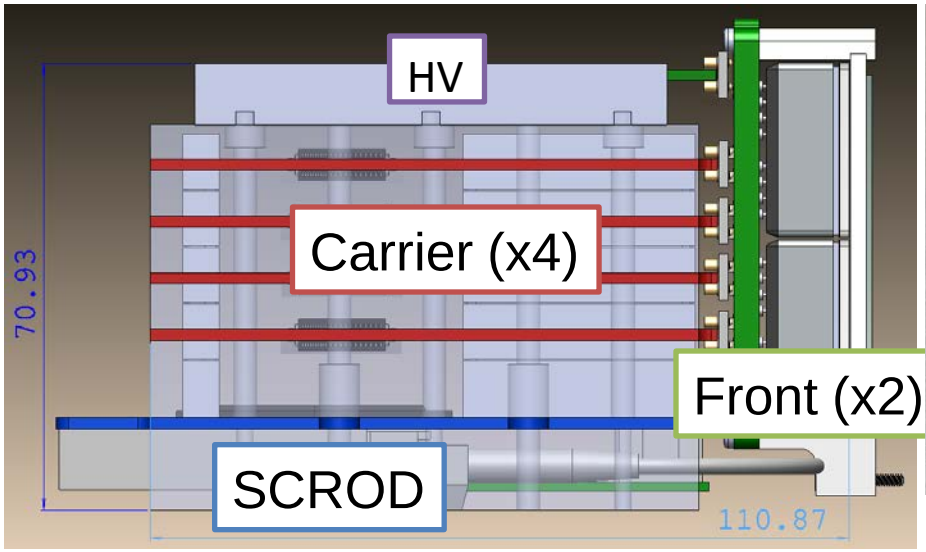
Electronics

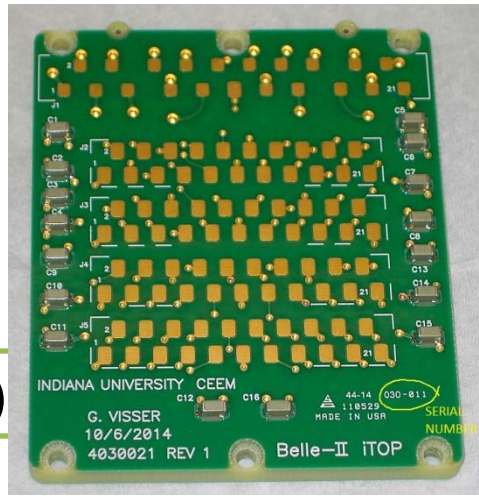


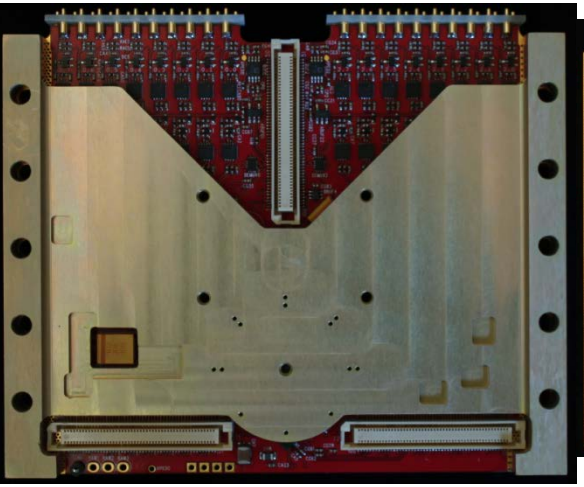
iTOP Readout “boardstack”

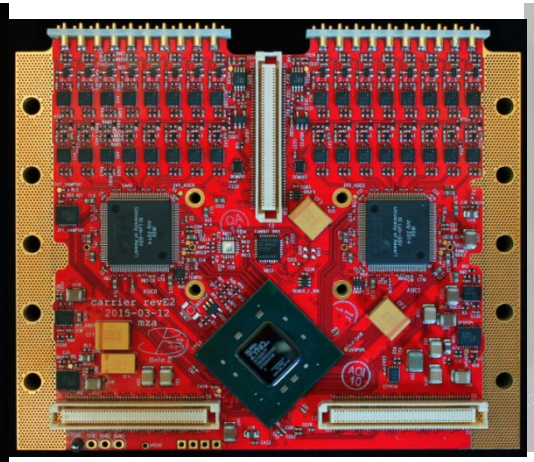
(1 of 4 per TOP Module)

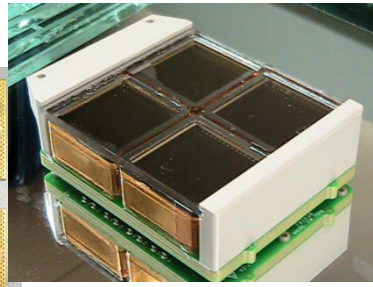




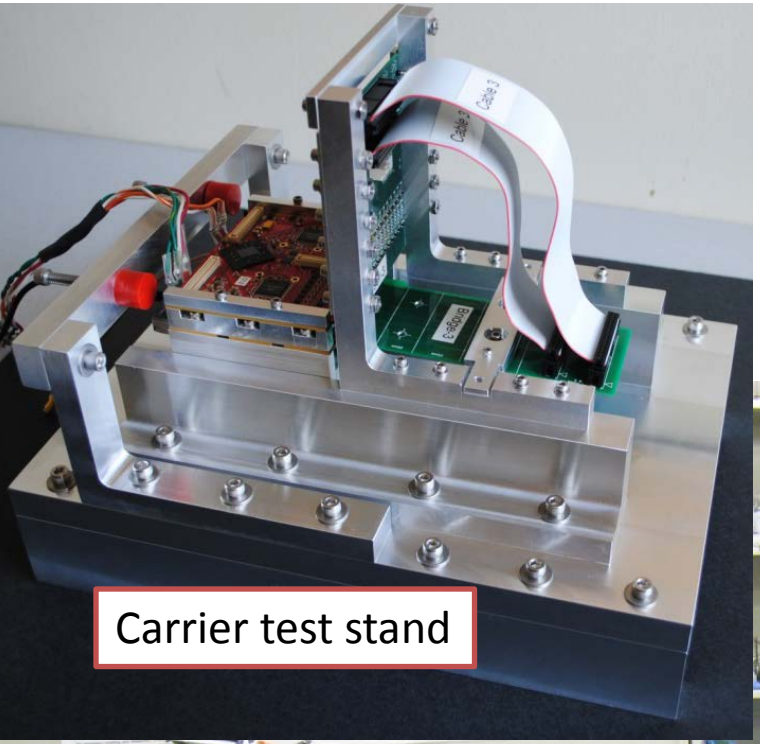




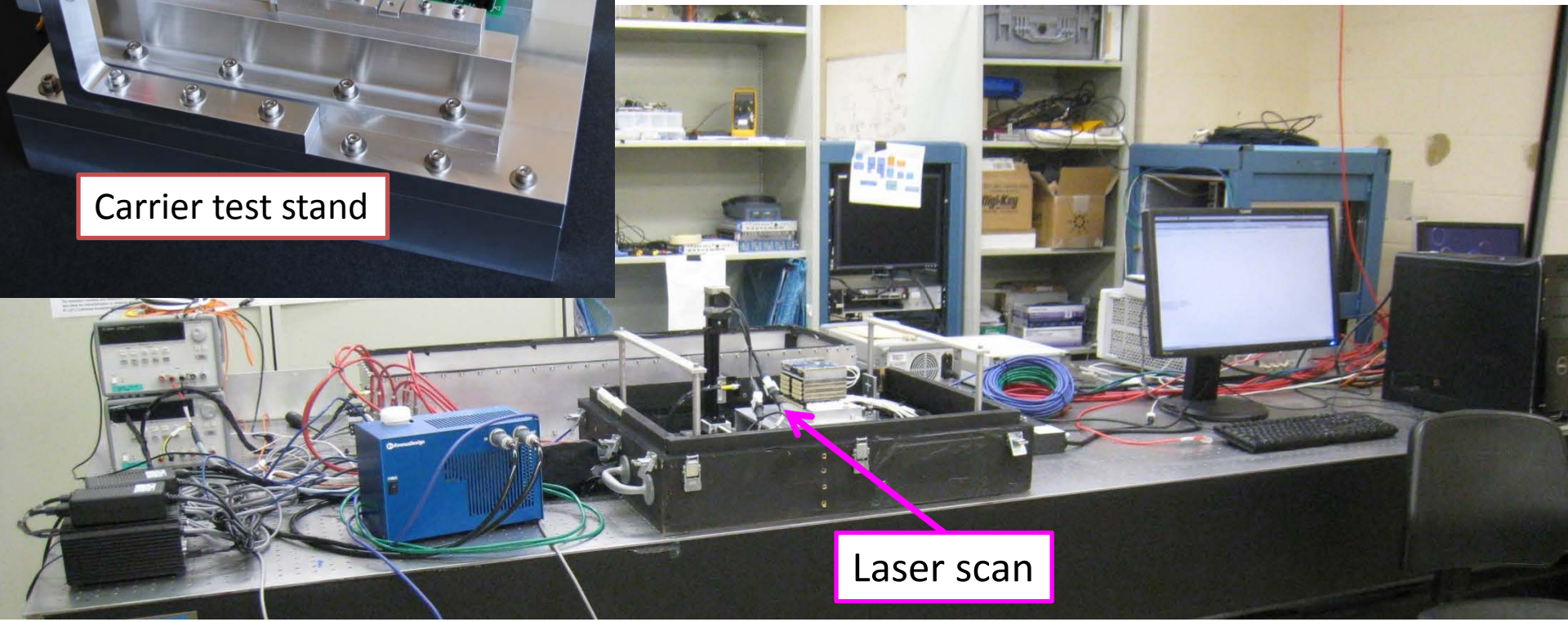




Test Stations

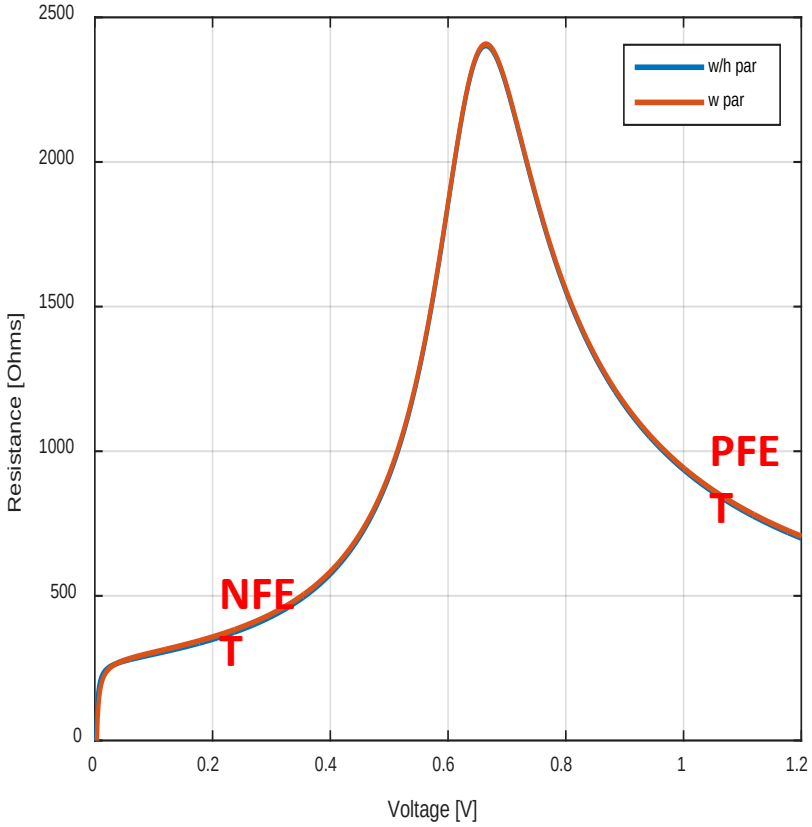


- 2x Carrier test stations at South Carolina, 1x backup in Hawaii
- Laser test stand Hawaii
- SCROD test stand in Pittsburgh
- Firmware test at PNNL



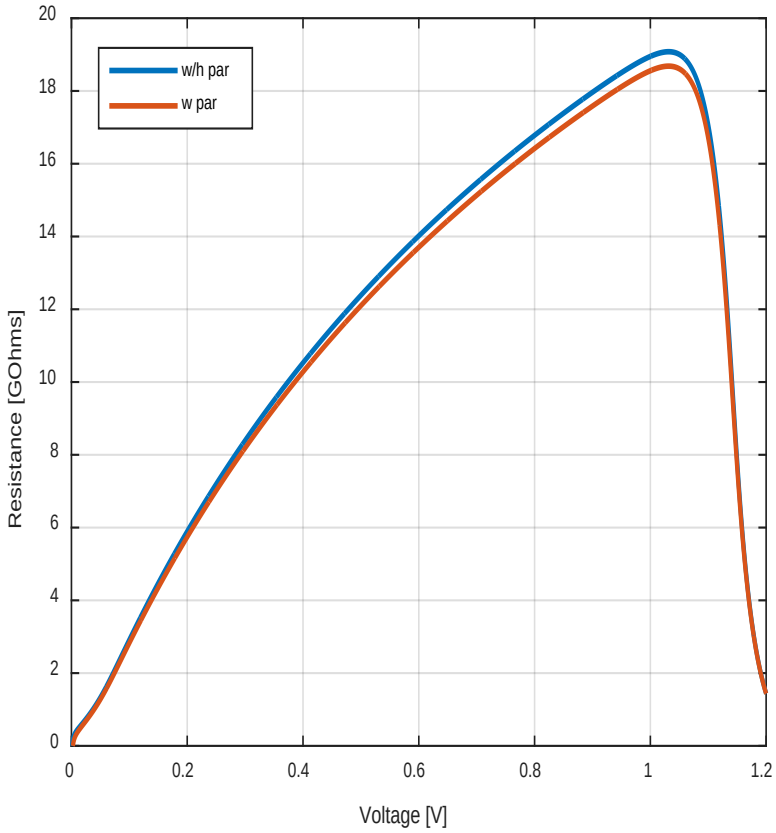
Pass Transistor (Switch) Resistance

TRACK state



- **Ron=2.4k @665mVdc**

HOLD state

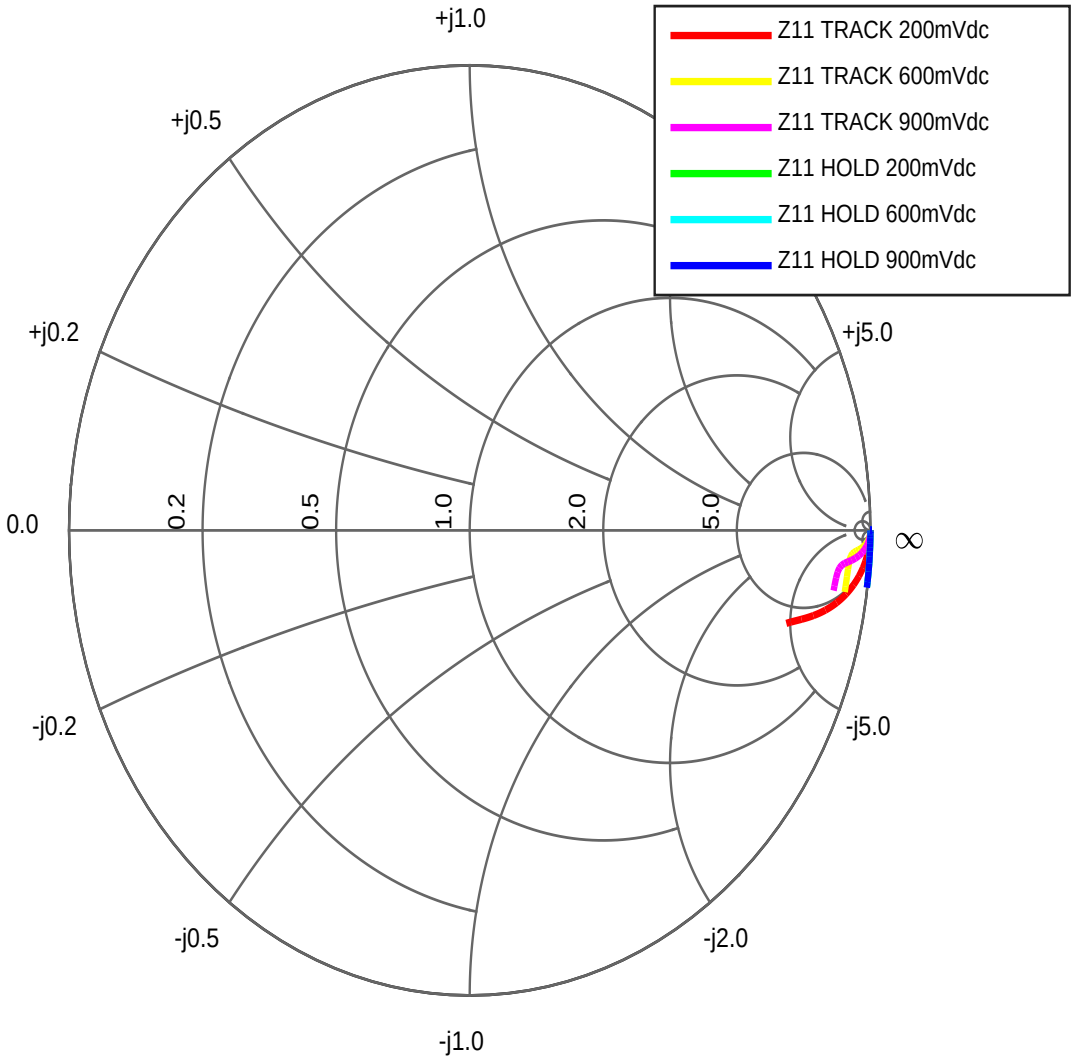


- **Roff is in GΩ**

- **The PFET and NFET are not matched and Ron varies considerably**

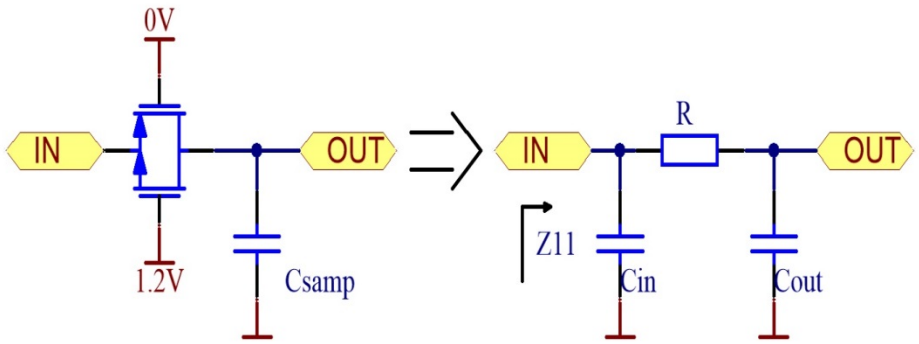
Frequency Analysis

Performance: S(Z)-parameter



The input impedance is high and it is capacitive.

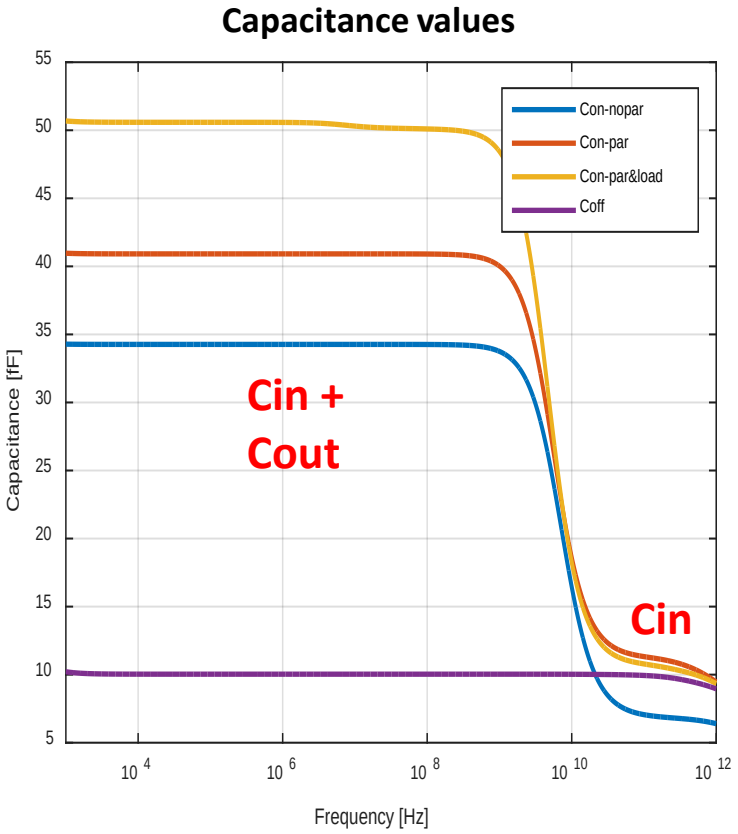
Input coupling analysis



$$Z_{11} = \frac{1 + sC_{OUT}R}{s^2C_{IN}C_{OUT}R + s(C_{IN} + C_{OUT})}$$

The transfer function parts:

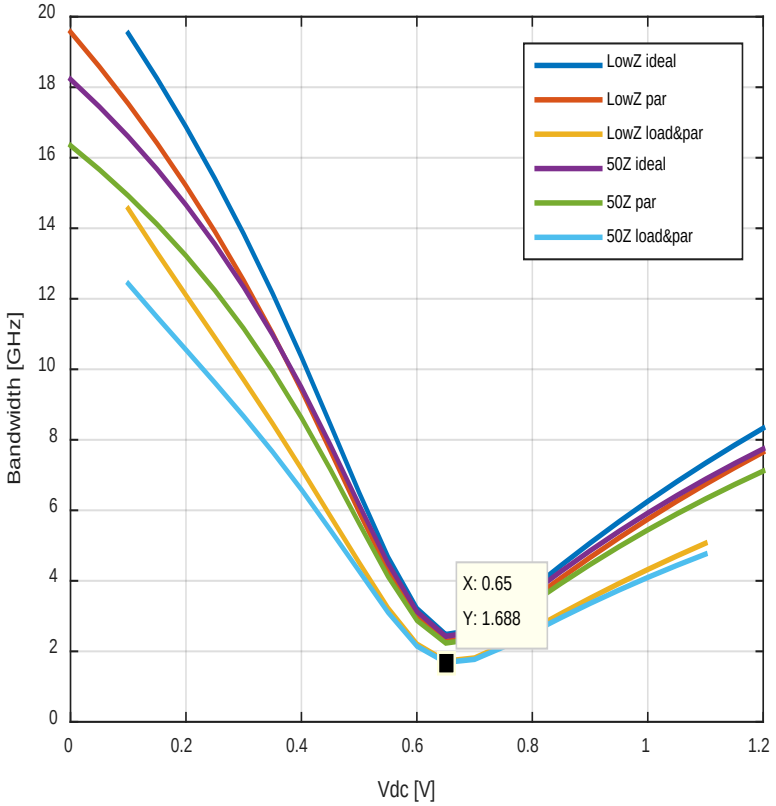
- input parasitic capacitance of the transistor plus capacitance of the transmission line section.
- Series resistance of the transistor channel (Rds)
- Output capacitance which is formed of the parasitic capacitance of the transistor, sampling capacitor and load capacitance



Capacitance	Value [fF]
Cin_open	8fF
Csw_out	10fF
Csamp	20.3fF
Cload	13fF

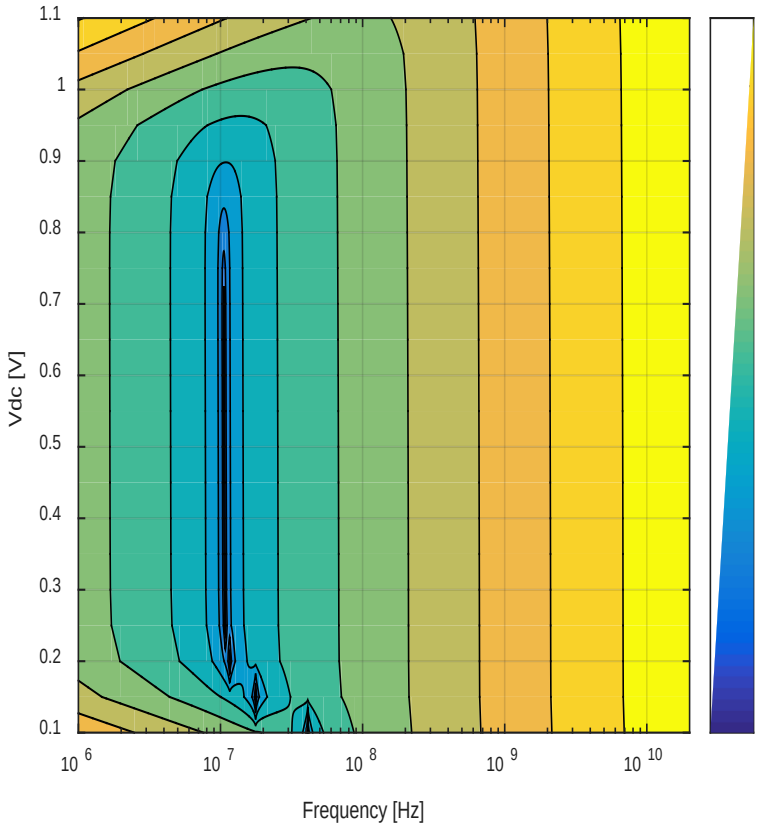
Small signal frequency response

Bandwidth



- BWworst≈2.3GHz @665mVdc @LowZ drive
- BWworst≈1.7GHz @665mVdc @50Ω drive

Isolation



- Isolation is over 60dB over all parameter space