JAVIER CARAVACA, BENJAMIN LAND, GABRIEL OREBI GANN

ELECTRONIC REQUIREMENTS FOR THEIA R&D AT BERKELEY

A TOUR FOR THEIA R&D AT BERKELEY

Veto panel

Veto panels underneath

1) Timing setup

Cherenkov/Scintillation
separation from vertical cosmics

12 1inch-PMTs H11934

2) Light setup

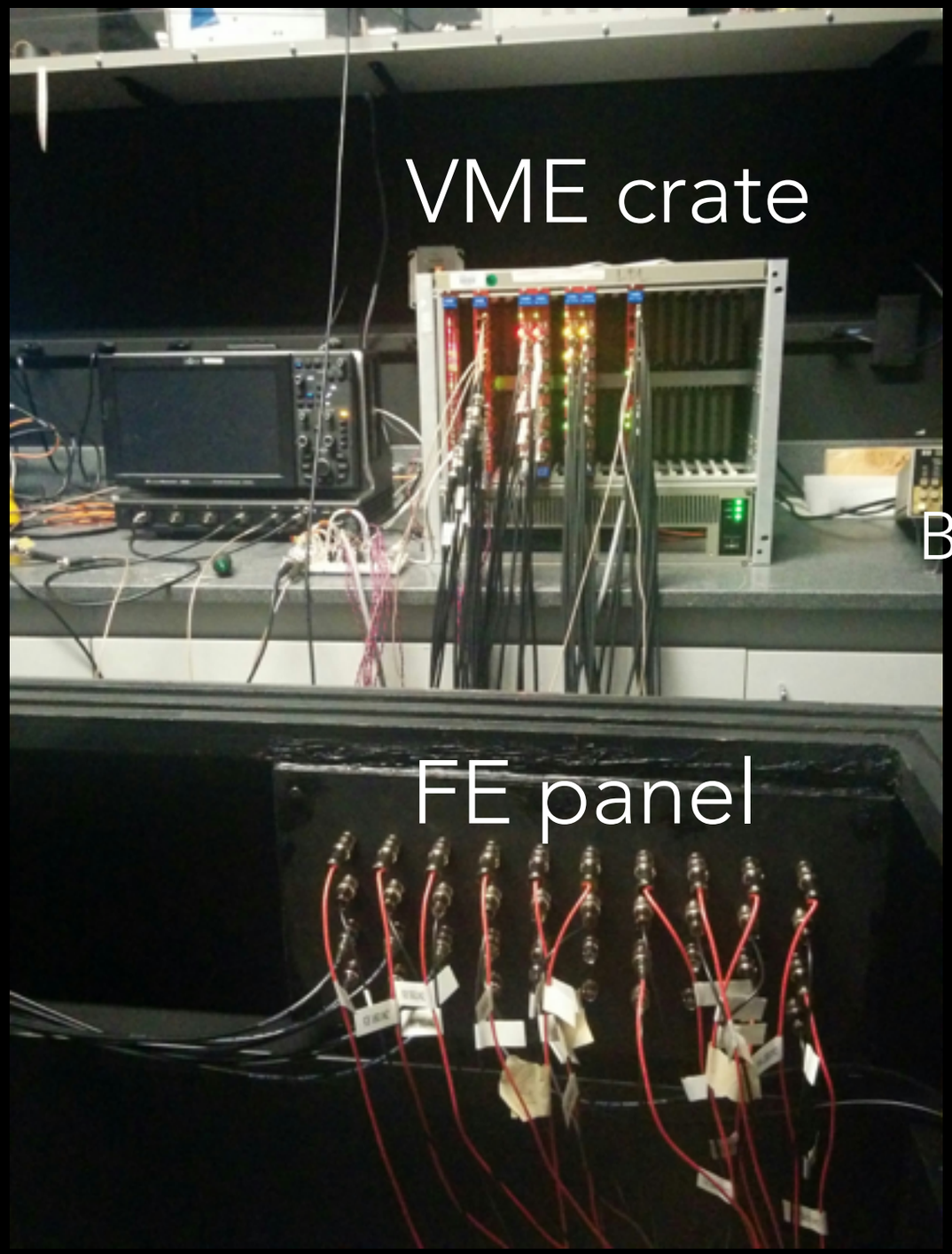
Measures the scintillation
light yield

6 10inch-PMTs R7081

FE panel

Veto panel

A TOUR FOR THEIA R&D AT BERKELEY



1) Timing setup

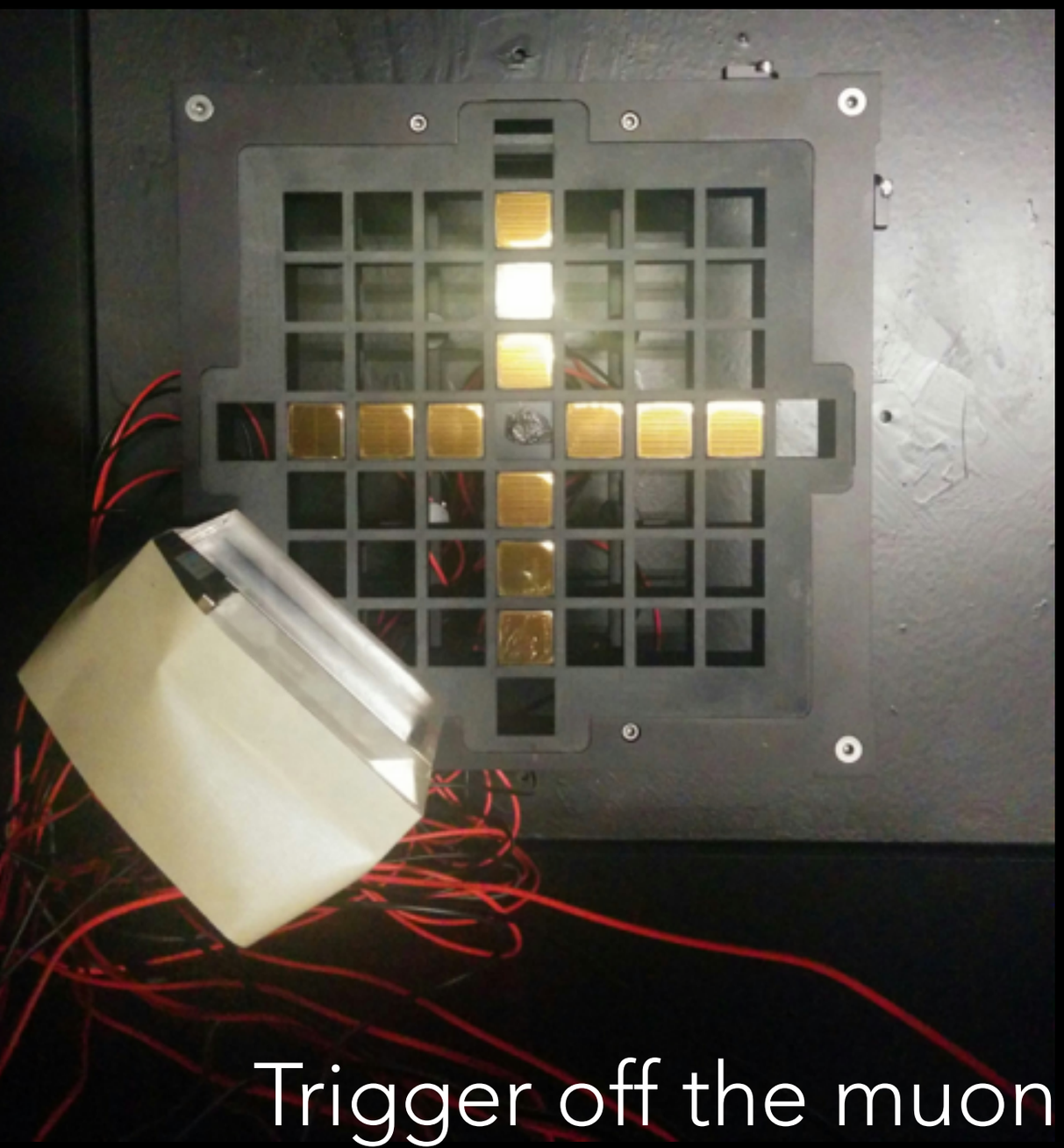
CAEN digitizer V1742 (5GHz)

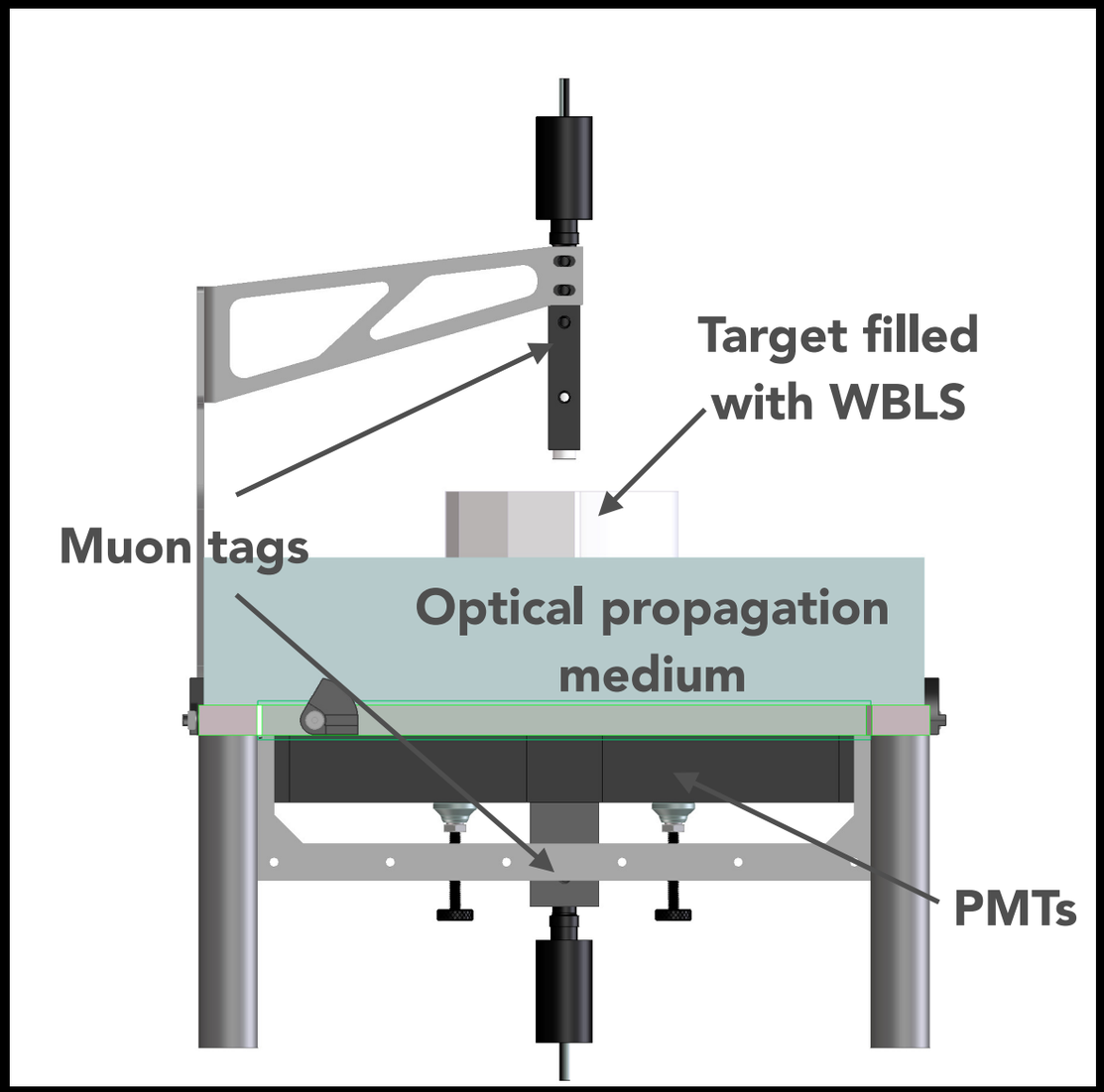
Buffer limited to 1024 samples → ~200ns event window

2) Light setup

CAEN digitizer V1730 (500MHz)

THE TIMING SETUP

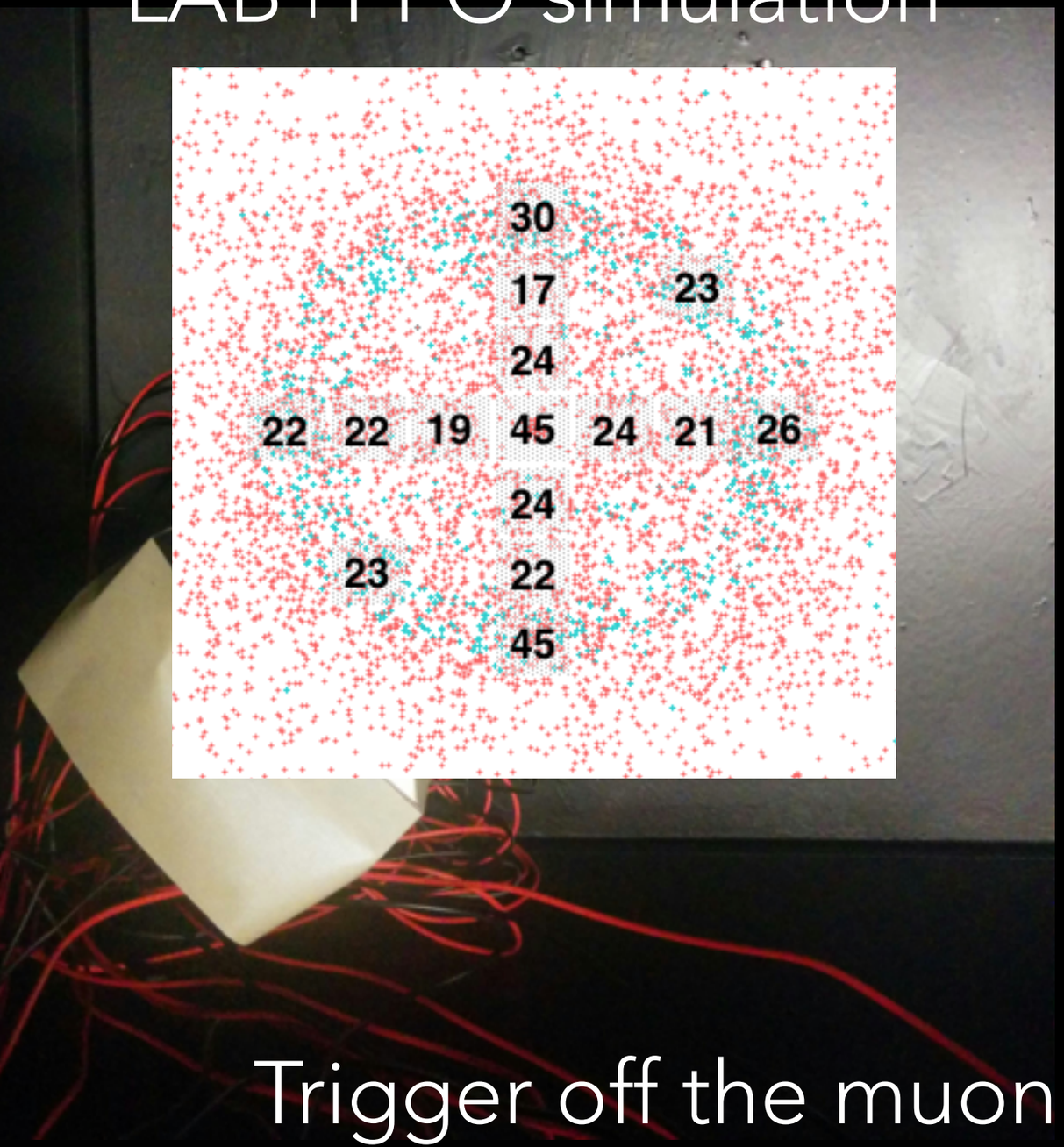


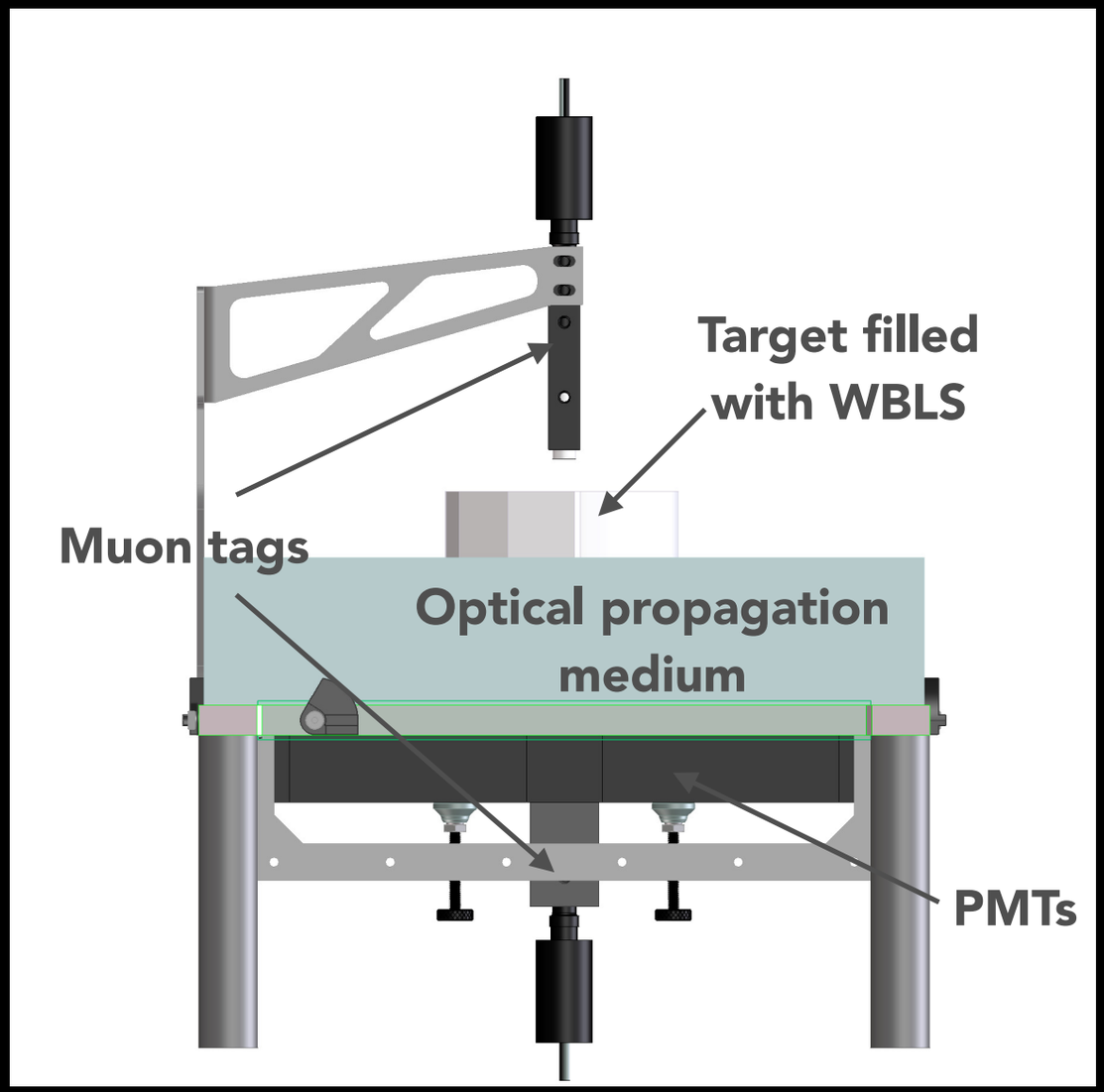


Trigger off the muon tags on vertical cosmics

THE TIMING SETUP

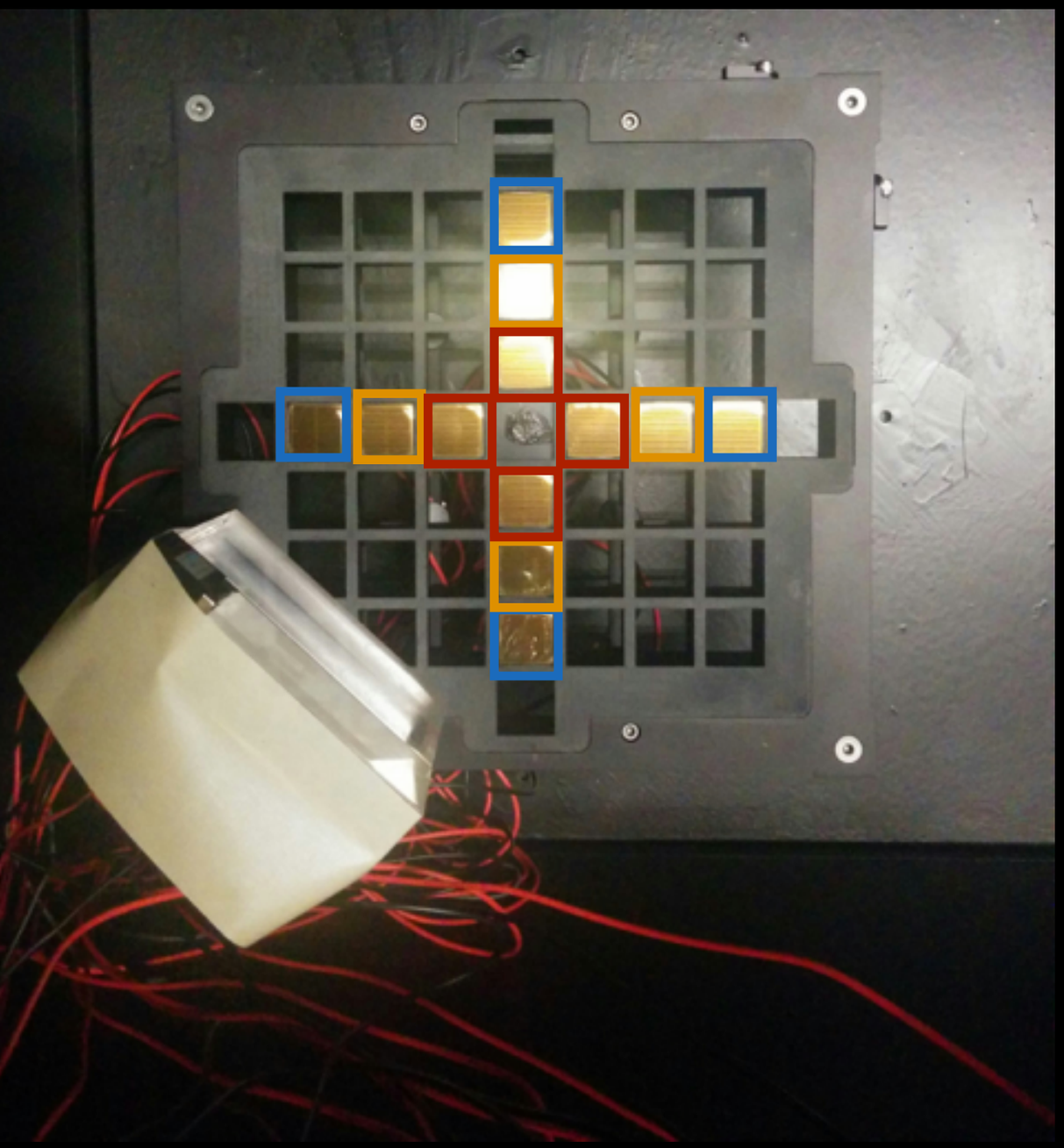
LAB+PPO simulation



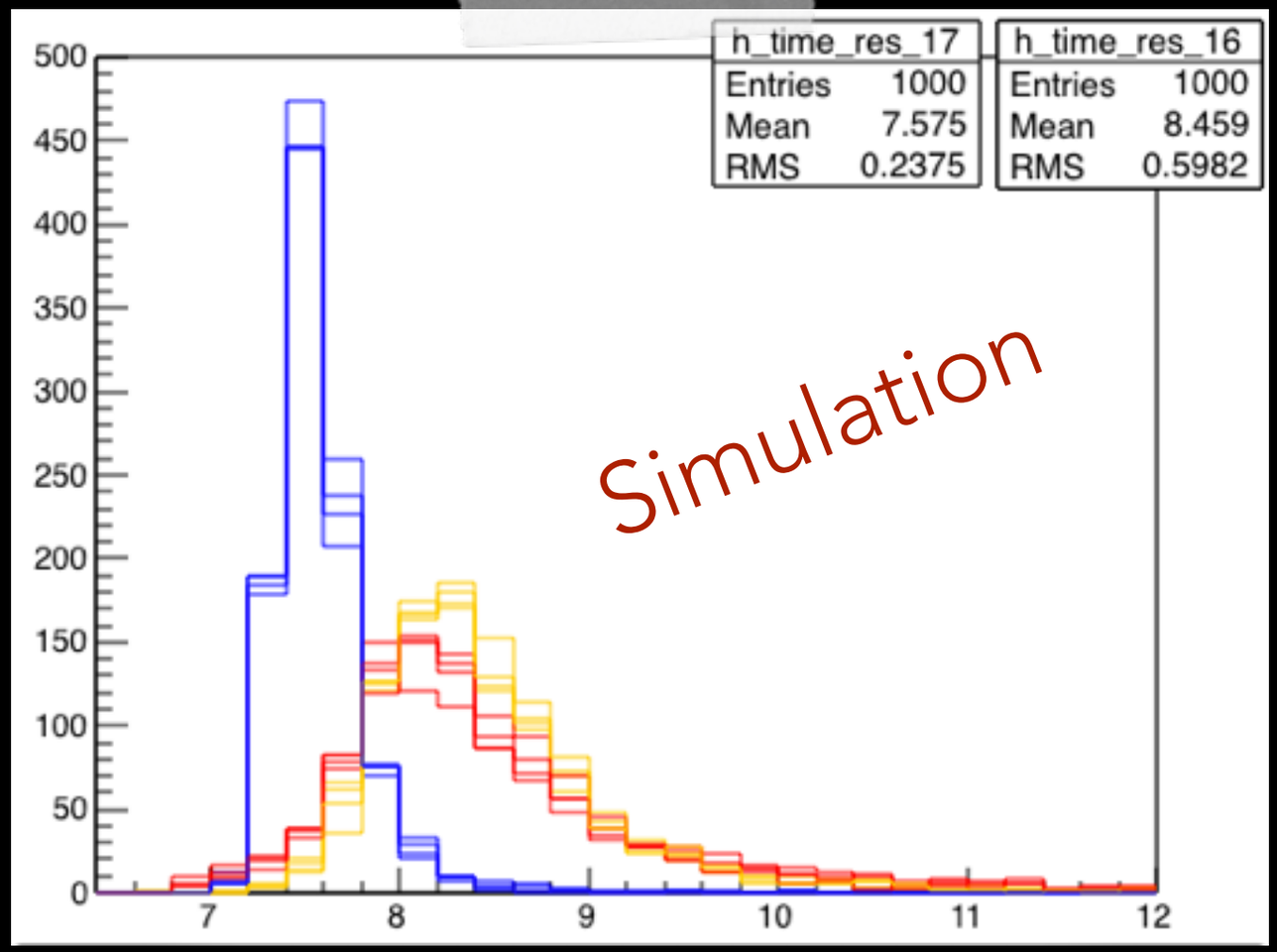


Trigger off the muon tags on vertical cosmics

PROJECTED PERFORMANCES OF OUR CURRENT SETUP



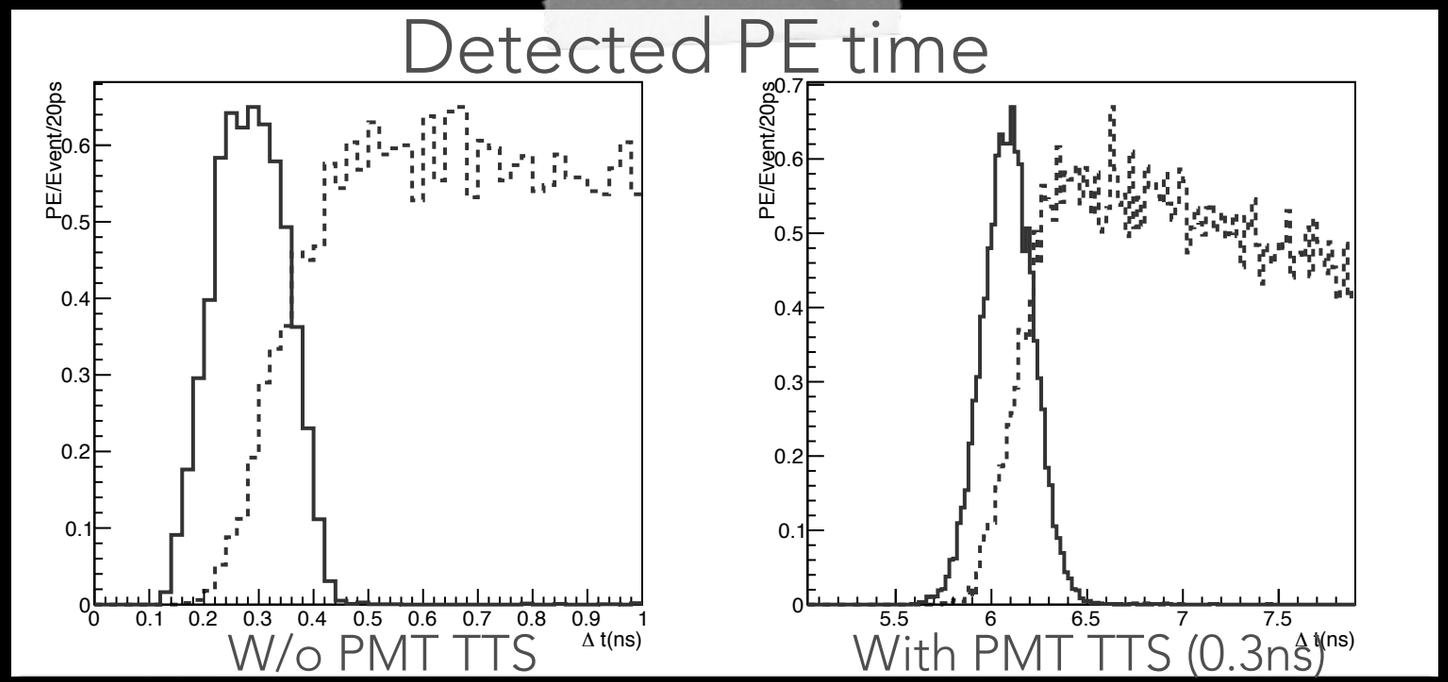
LAB+PPO



Detected PE time, ToF corrected (ns)

Simulation includes most of the DAQ effects → PMT TTS, realistic pulses, electronic noise, …

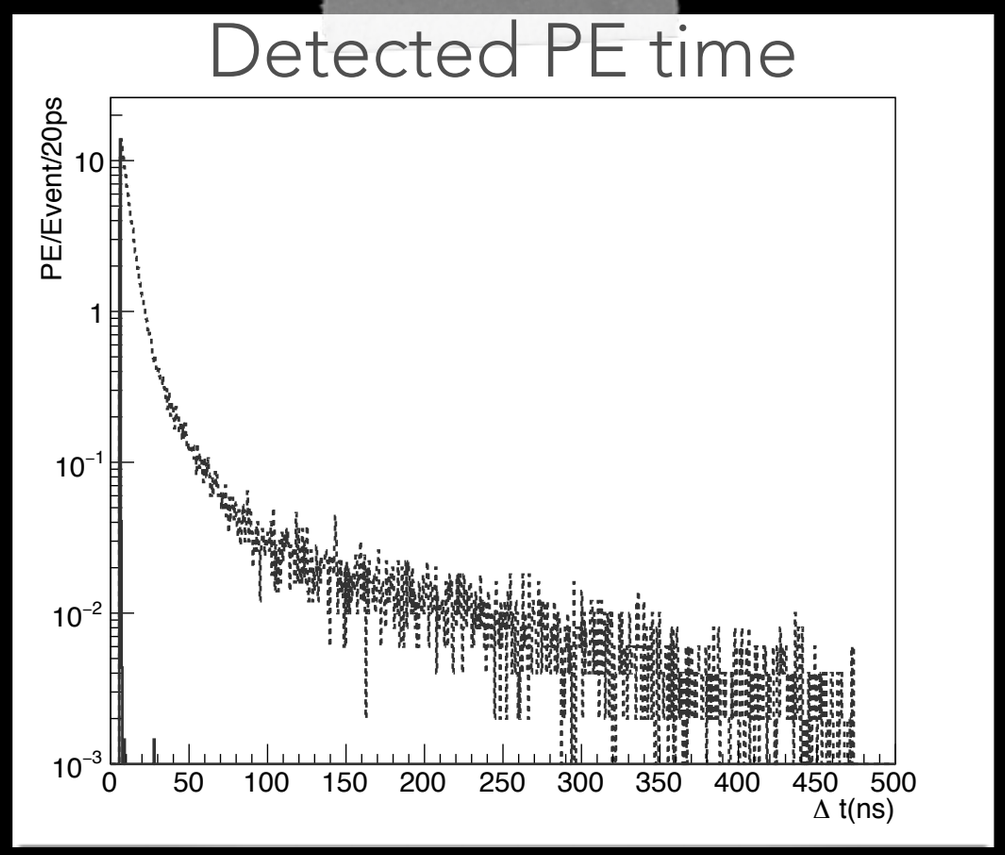
CHERENKOV VS SCINTILLATION



Solid - Cherenkov

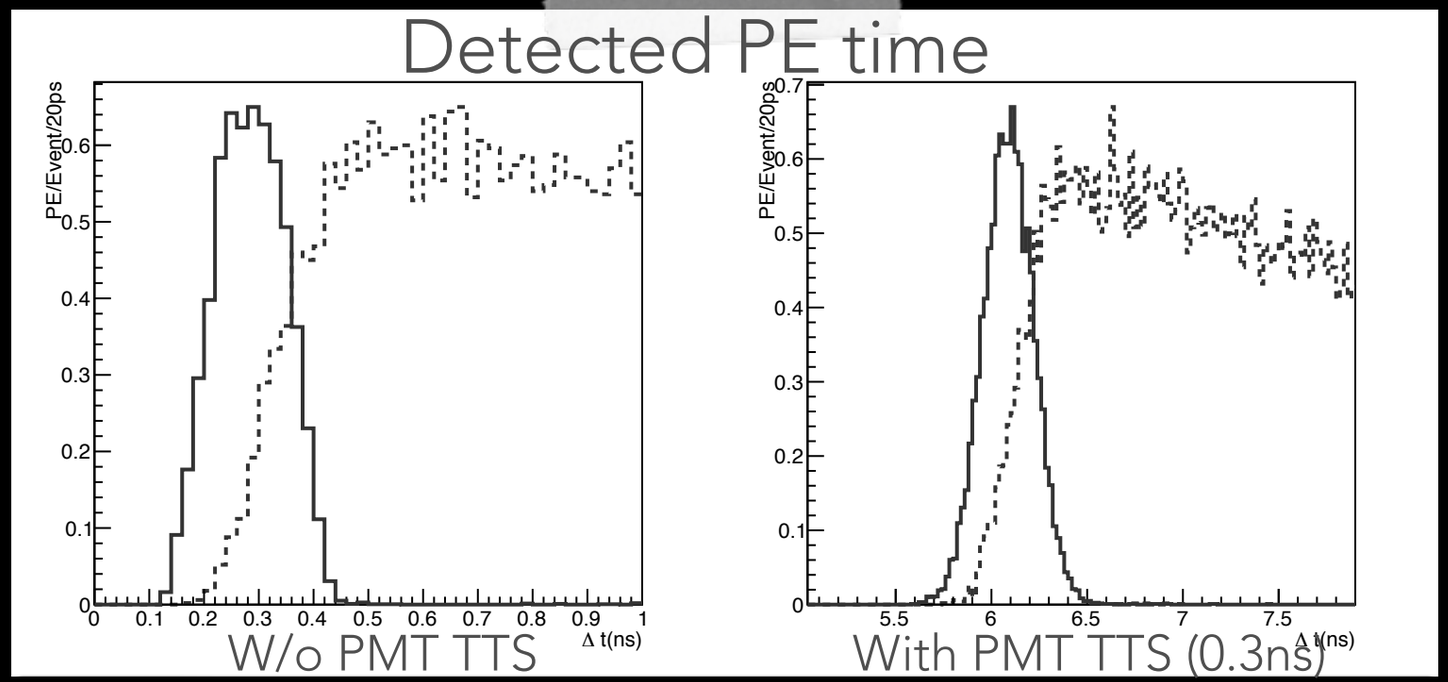
Dash - Scintillation

Typically <ns difference



Scintillation tails extends to ~400ns

CHERENKOV VS SCINTILLATION



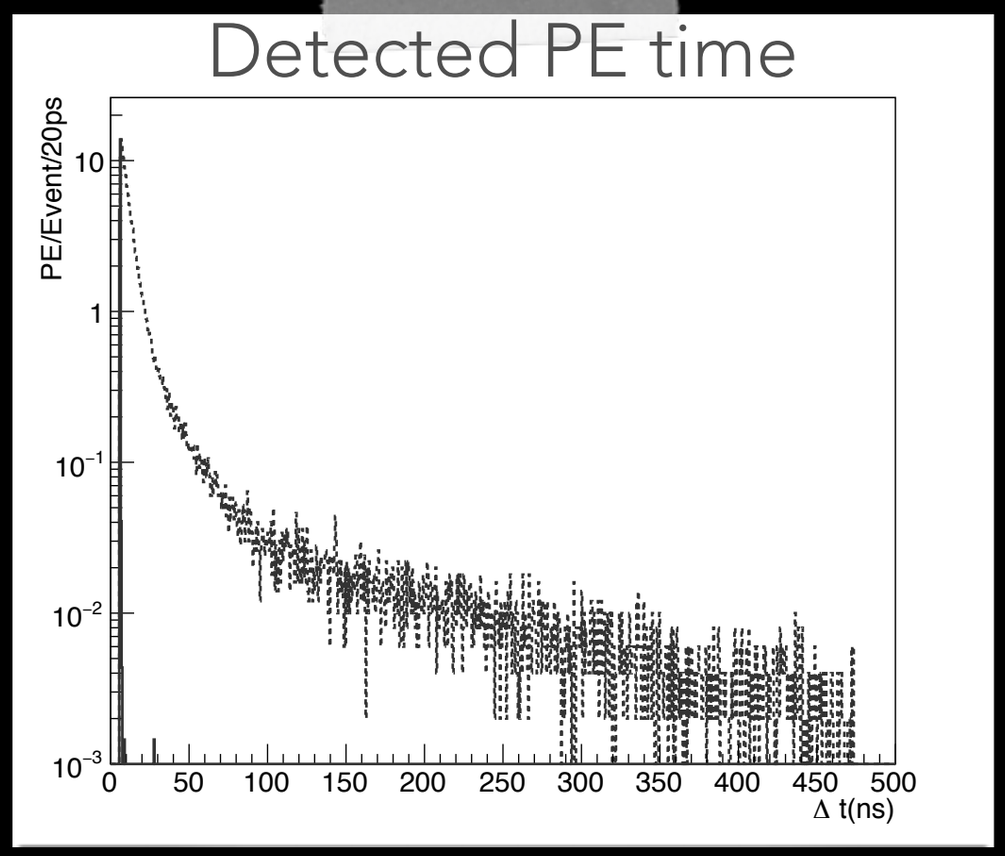
Solid - Cherenkov

Dash - Scintillation

Typically <ns difference

Fast sampling rate

~10GHz (0.1ns)



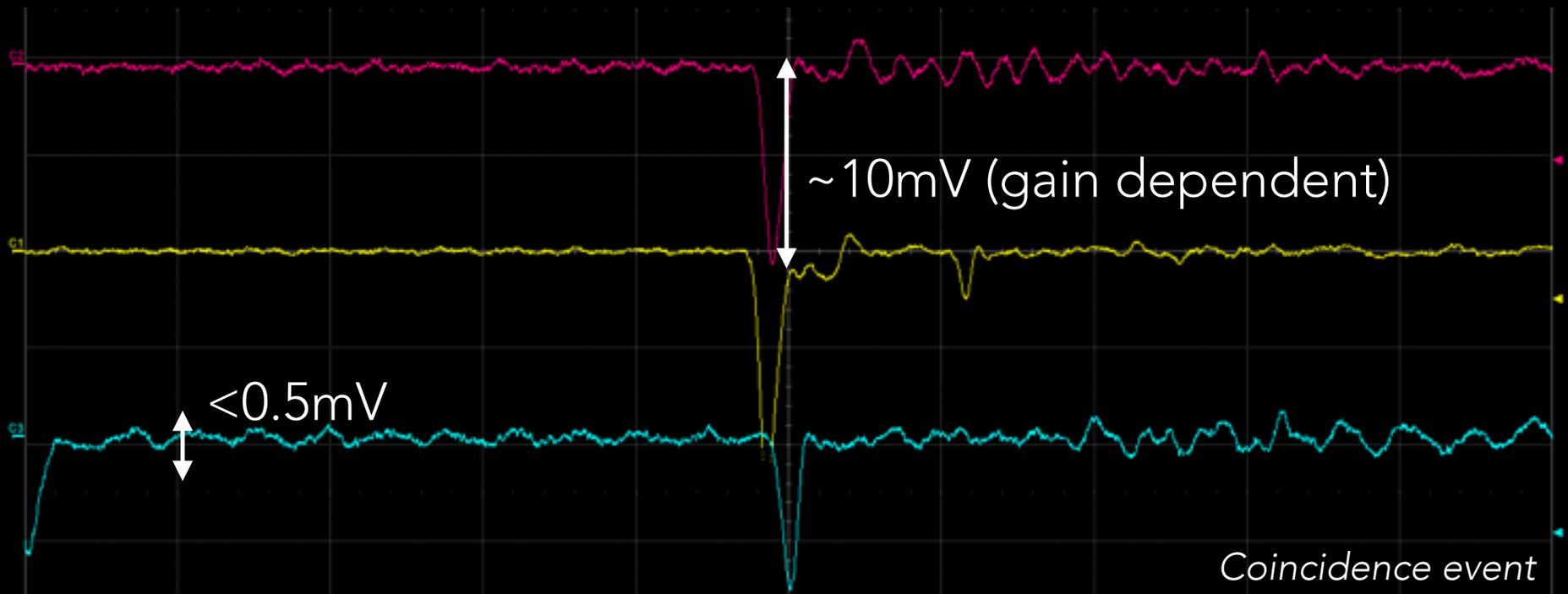
Scintillation tails extends to ~400ns

Large buffers > 400ns

CRITICAL POINTS

- **Sampling rate**
  - Currently working at 5GHz → 0.2ns resolution
  - The current limiting factor is the PMT TTS ~ 0.3ns
    - Getting to 0.1ns would neglect the source of error coming from the electronics
- **Buffer size**
  - Not catching the whole scintillation light (~400ns) would lead to systematics in the light yield measurements
  - Preferably larger than 400ns to allow for direct pedestal correction

DYNAMIC RANGE



- Handling single and multi PE at a time requires a broad range with a good enough resolution
- A 2V range with 12 bits resolution (0.5mV) has demonstrated to be sufficient

TRIGGERING CAPABILITIES

- **Customizable global trigger**
  - Issue from any of the channels
  - Coincidence & anti-coincidence from two or more channels
  - Rising or falling edges
  - Configurable threshold
  - On-board pedestal correction
- **Trigger delay:** useful for synchronization with external triggers
- **Clock**
  - Synchronization capabilities: for event correlation between devices
  - Timestamp rollover>hours → 50bit 10GHz would be ideal

SUMMARY

- Fast digitization is crucial for this project as well as a large enough buffer

- Scalability is a plus → Currently using 25 channels. Might be extended to >30.

- **Requirements**

Factor	Min. Required	Preferred	Max. Desired
Sampling Rate	5 GHz (0.2 ns)	10 GHz (0.1 ns)	10 GHz (0.1 ns)
Dynamic Range	1 V (fully negative)	2 V (offset ±2 V)	5 V (offset ±5 V)
Voltage Resolution	1 mV (11 bits)	0.5 mV (12 bits)	0.1mV (14 bits)
Timestamp Clock	10 MHz (offset)	100 MHz (offset)	10 GHz (latch on trigger)
Timestamp Rollover	hours (41 bits)	days (46 bits)	days (46 bits)
Buffer Size (per event)	400ns (4000 samples)	1 us (10k samples)	10 us (100k samples)